Building a quantum computer using quantum dots in silicon

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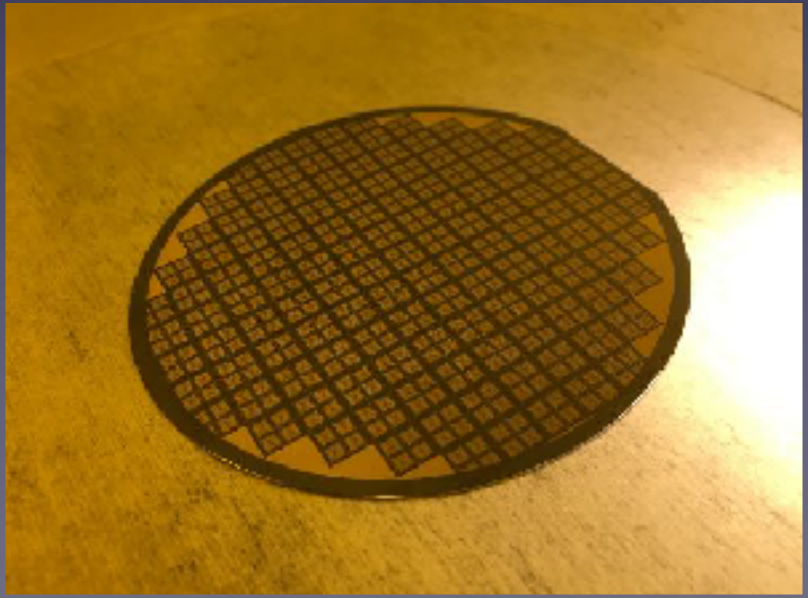
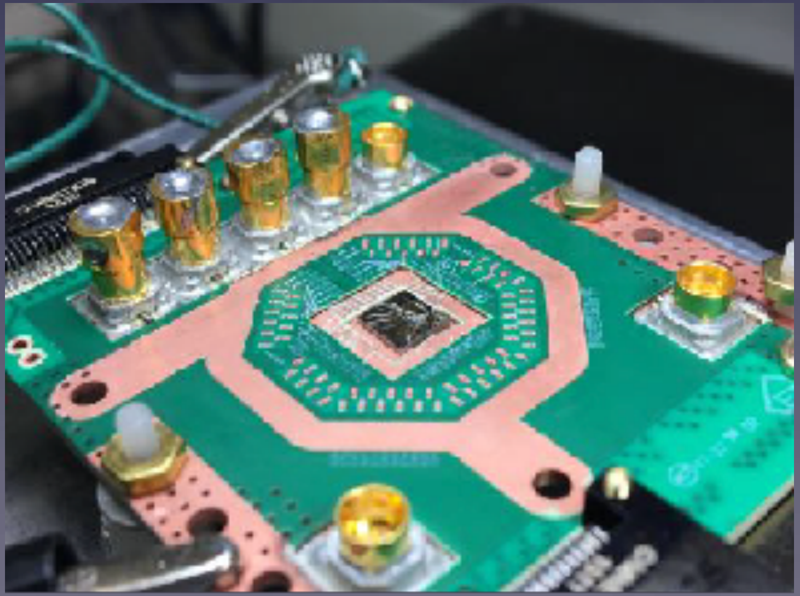
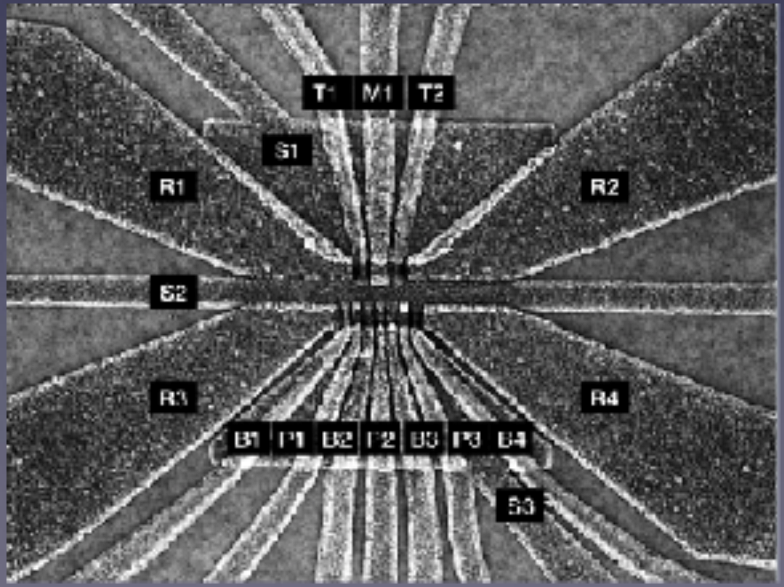


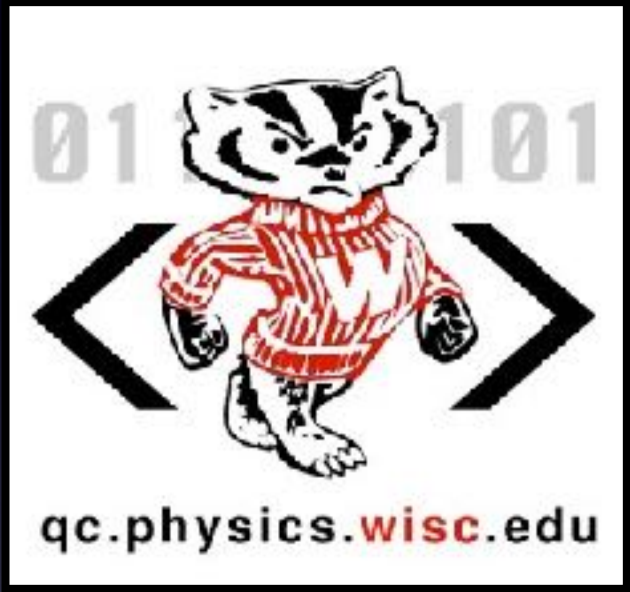




UW-Madison Solid-State Quantum Computing Team

PI: Mark Eriksson

Sam Neyens, Ryan Foote, Brandur Thorgrimsson, Trevor Knapp, Evan MacQuarrie, Nathan Holman, Joelle Baer, JP Dodson, Tom McJunkin, Don Savage, Max Lagally



SNC theory collaborators:

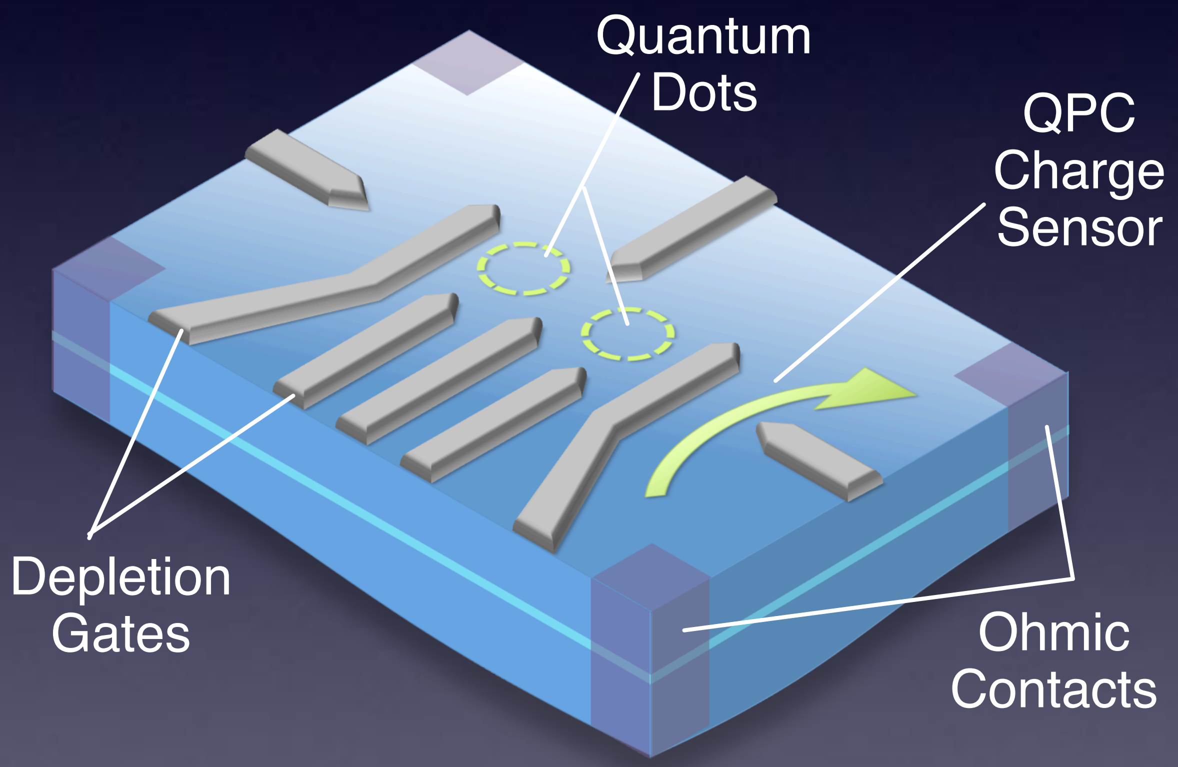
Mark Friesen

Yuan-Chi Yang, Joydip Ghosh, Ekmel Ercan, Adam Frees, Cameron King, John Gamble, Viktoriia Kornich, Robert Joynt

Sponsored in part by the Army Research Office, the Office of Naval Research, the Department of Energy, the National Science Foundation, and the United States Department of Defense.

UW Si/SiGe quantum dot quantum computer

Overview of our approach: quantum dots in Si/SiGe heterostructures confined and controlled with voltages applied using top gates



Voltages applied to top gates define electron potentials. Conductance through quantum point contact (QPC) depends on dot occupancies.

D. Loss and D.P. DiVincenzo, Phys. Rev. A 57, 120 (1998)

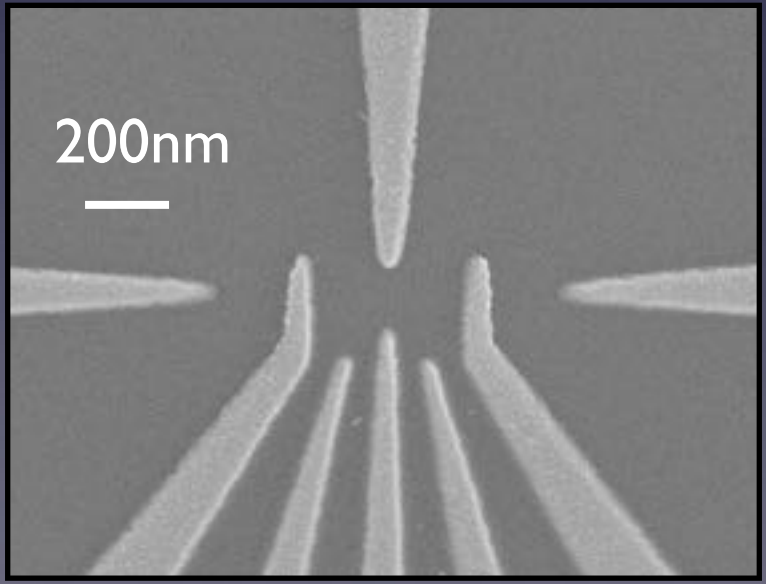
Why make qubits using silicon quantum dots?

Fabrication techniques similar to those used in (classical) electronics

→ Plausible path to large-scale scalability

→ Plausible path to integration with large-scale classical electronics

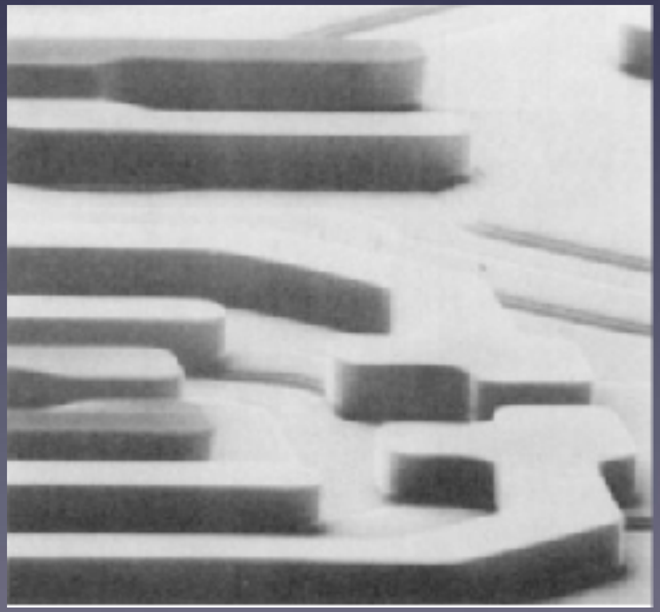
double quantum dot qubit



metal gates on semiconductor

D. Kim et al., *Nature* **511**, 70-74 (2014).

classical transistor



distance between features ~1μ

metal gates on semiconductor

Frontiers in Chemical Engineering: Research Needs and Opportunities (NRC, 1988)

Overview of current status of silicon quantum dot qubits:

Single-qubit gates:

>99.9% fidelity gates demonstrated experimentally

Y. Yoneda et al., Nat. Nano. 13, 102-106 (2018)

Theory predicts even higher fidelities are possible by increasing driving strength

Two-qubit gates:

CNOT fidelity >90%; Bell state fidelities ~80%

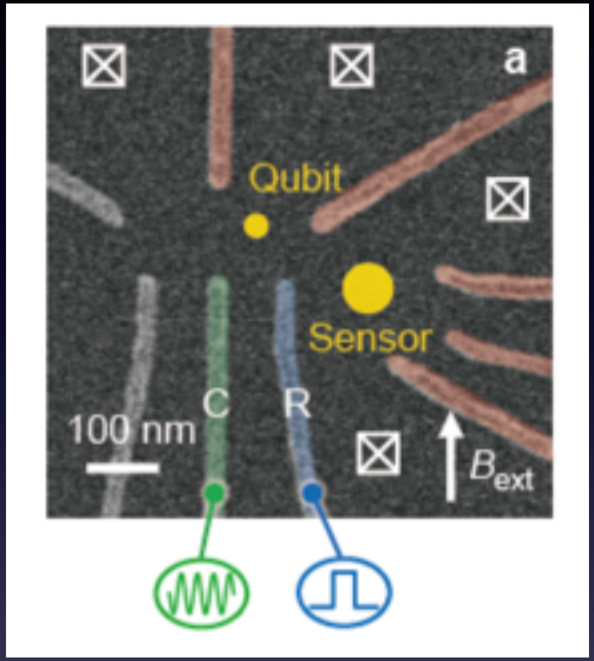
W. Huang et al., arXiv:1805.05027; D.M. Zajac et al., *Science* (2017); T. Watson et al., *Nature* **555**, 633 (2018)

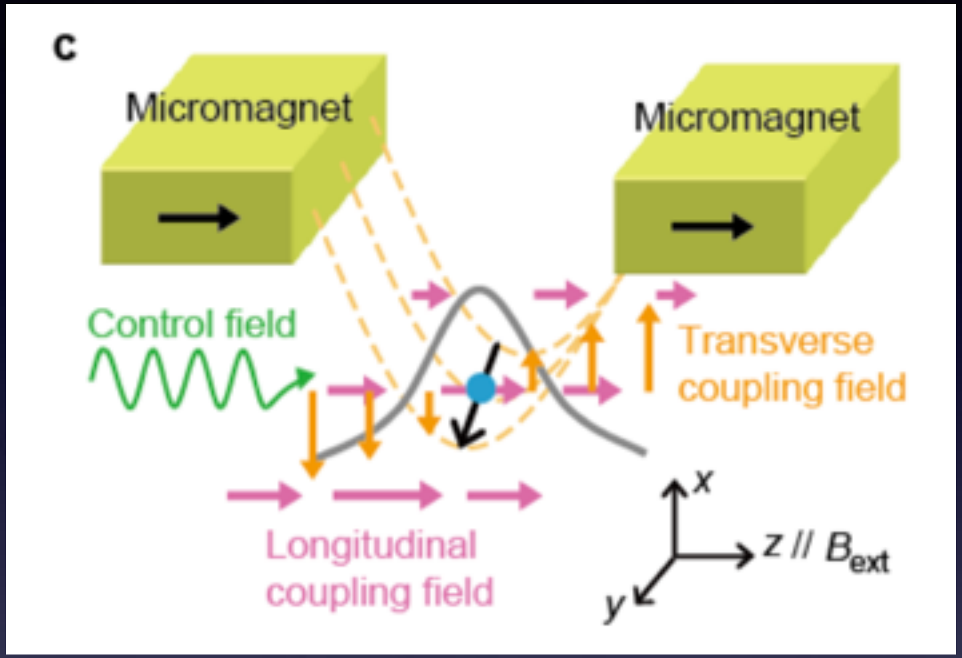
There are strong indications that higher fidelities are achievable

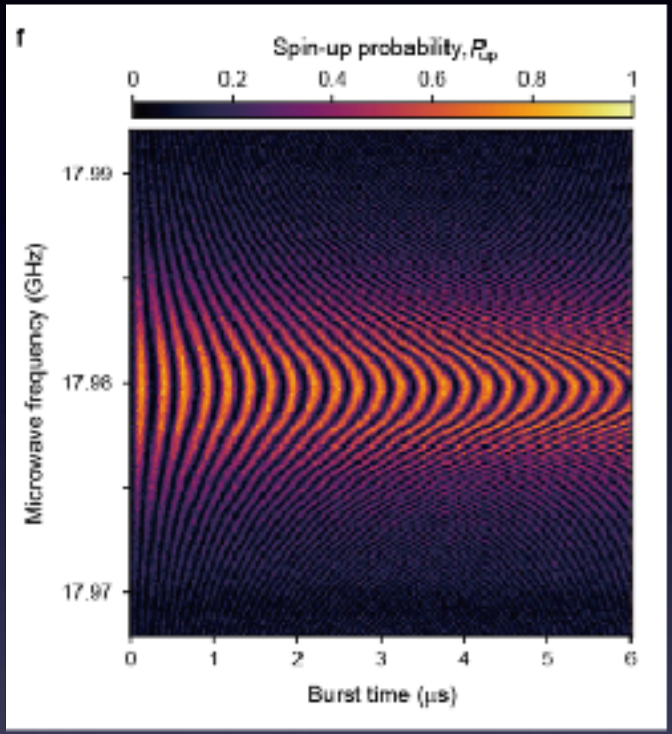
Single-qubit gates in silicon quantum dots

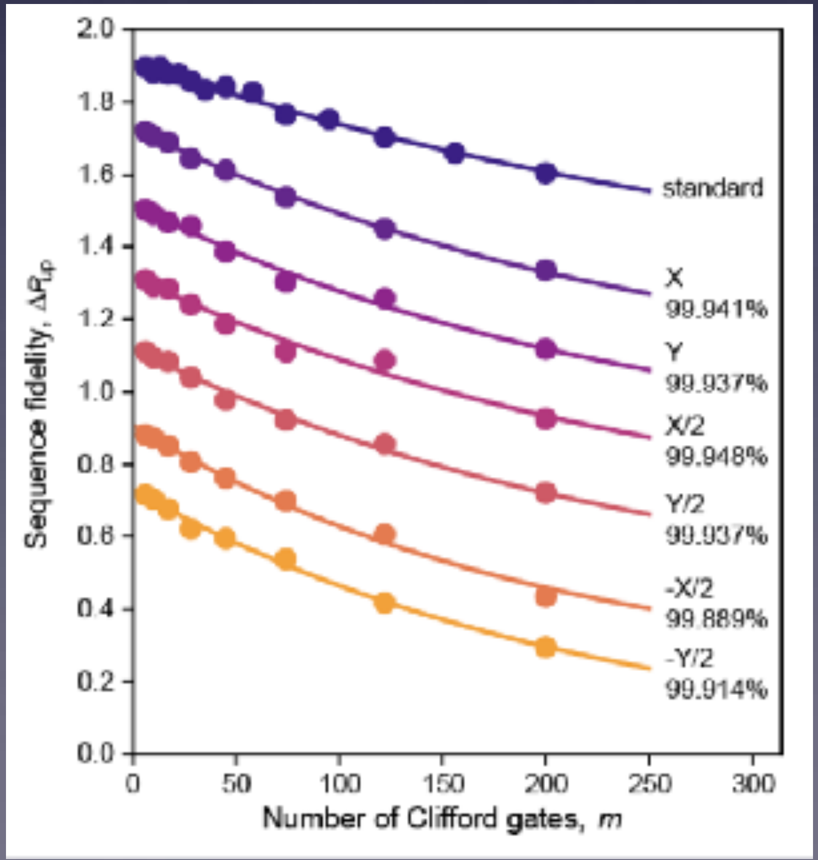
Several groups have demonstrated single-qubit gate fidelities >99%

Yoneda et al. (Tarucha, RIKEN/Tokyo) have reported single-qubit gate fidelities >99.9%.







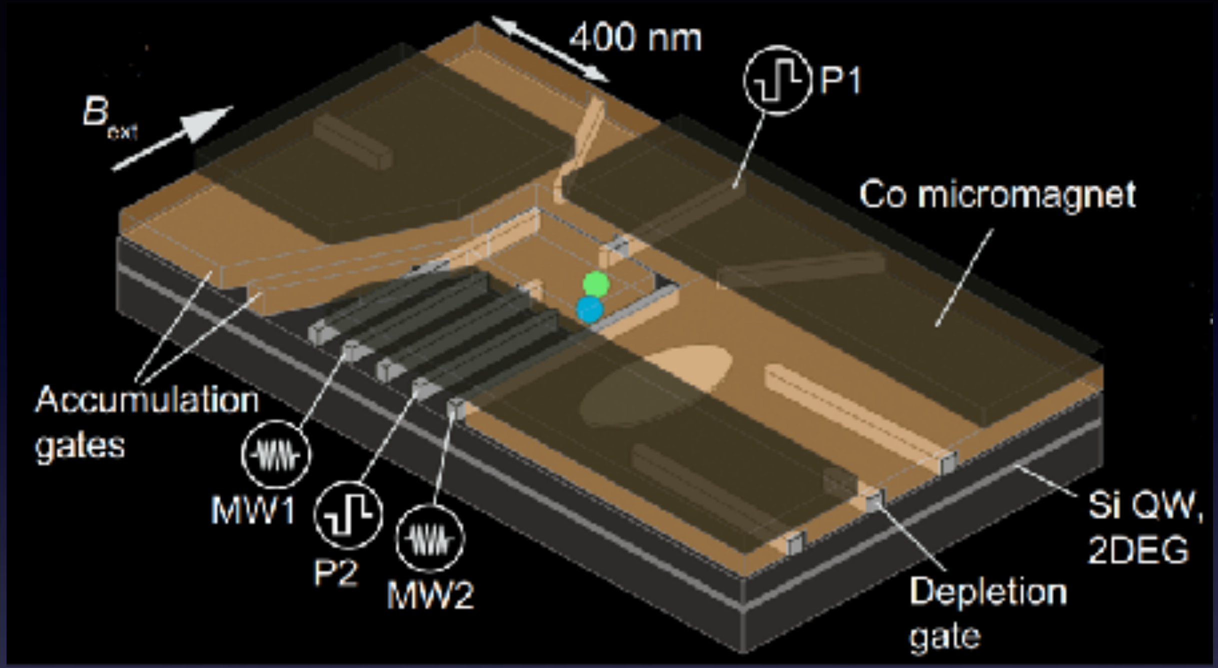


Single Clifford gate fidelity: 99.861± 0.005%
Average single gate fidelity: 99.926±0.002%
Average fidelity from randomized benchmarking: 99.928%

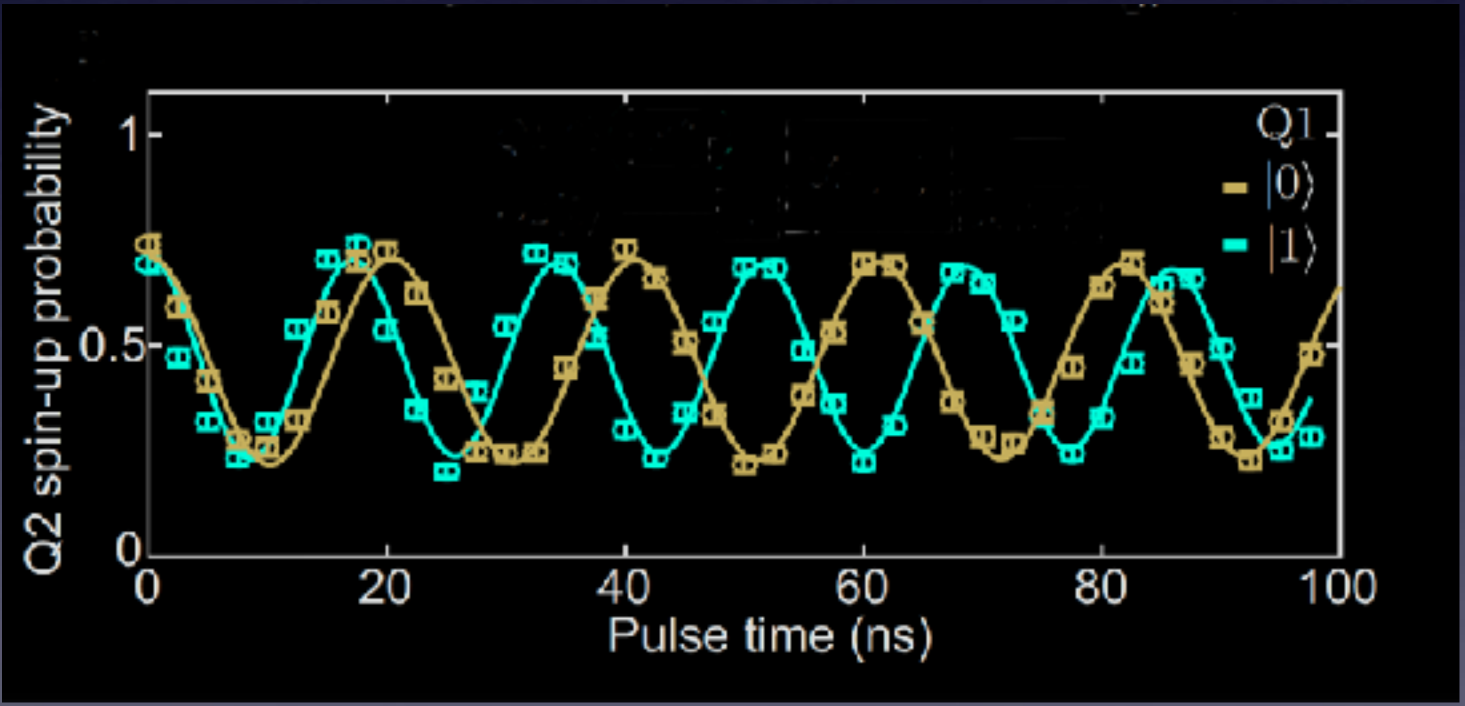
Y. Yoneda et al., Nature Nanotechnology 13, 102-106 (2018)

Two-qubit gates in silicon quantum dots

T. Watson et al., Nature **555**, 633 (2018) (Vandersypen, TU Delft and Eriksson, Wisconsin-Madison)



A two-qubit gate: rotation rate of the second qubit depends on the state of the second qubit, and vice versa.



Yellow: Rotations of Qubit 2 when Qubit 1 is in state |0⟩

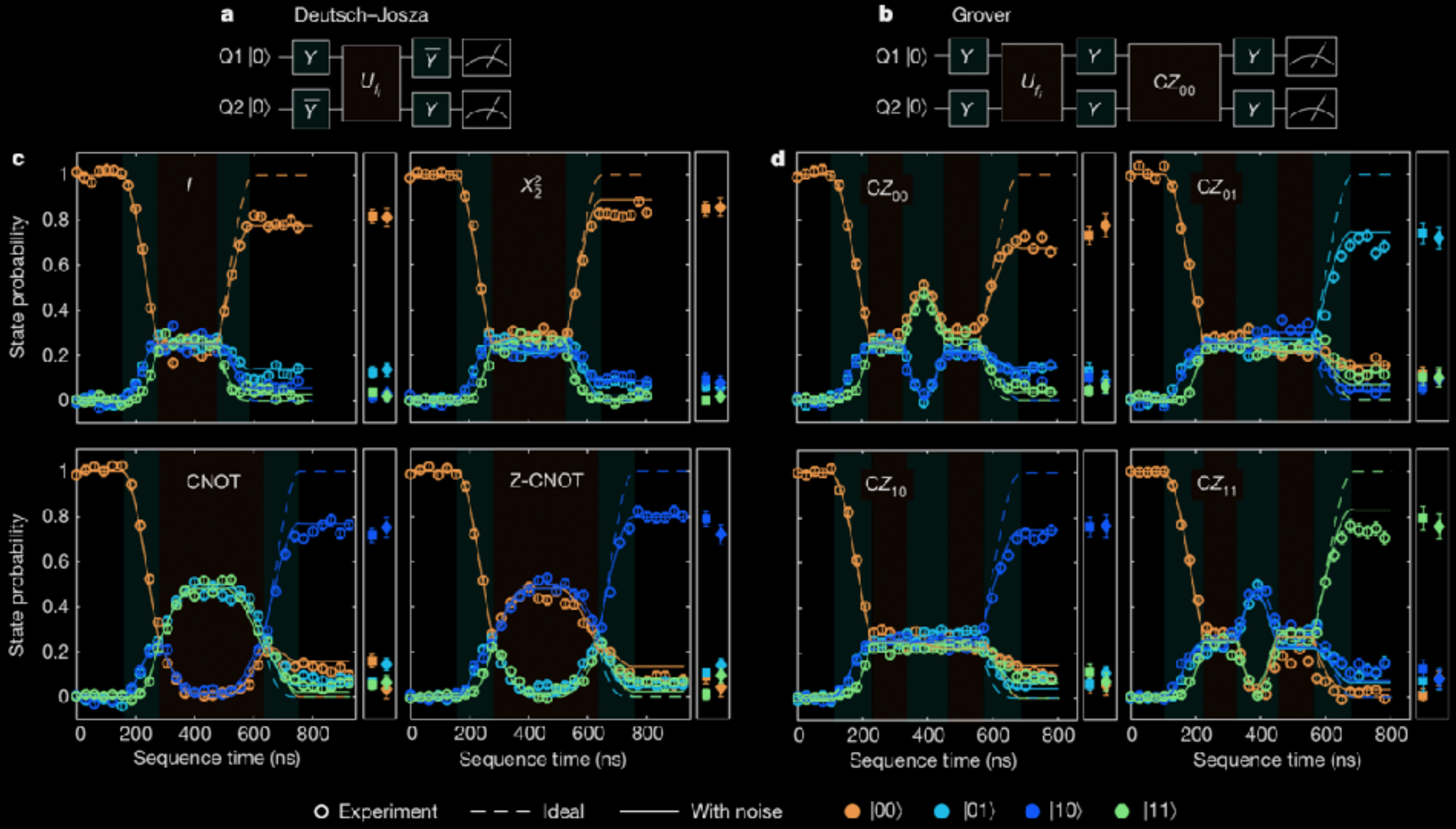
Aqua: Rotations of Qubit 2 when Qubit 1 is in state |1⟩

Bell state preparation

state	fidelity	concurrence
Ψ+	0.88±0.02	0.80±0.03
Ψ-	0.88±0.02	0.82±0.03
Φ+	0.85±0.02	0.73±0.03
Φ-	0.89±0.02	0.79±0.03

Quantum algorithms on a two-qubit processor in silicon

T. Watson et al., Nature **555**, 633 (2018)



Successful implementation of simple algorithms, but current two-qubit gate fidelities in Si are not yet good enough for scalable quantum computation. Dominant limitation is charge noise in the devices (but this is improving).

The field is progressing quickly, but the goal is challenging. Improving materials is crucial for making better silicon qubits.

Two examples:

- Understanding the effects of defects in Si metal-oxide-semiconductor devices
  - Impurities in the oxide can cause additional "impurity dots" that degrade performance
  - Problems can be mitigated both by improving materials and by changing gate designs. •

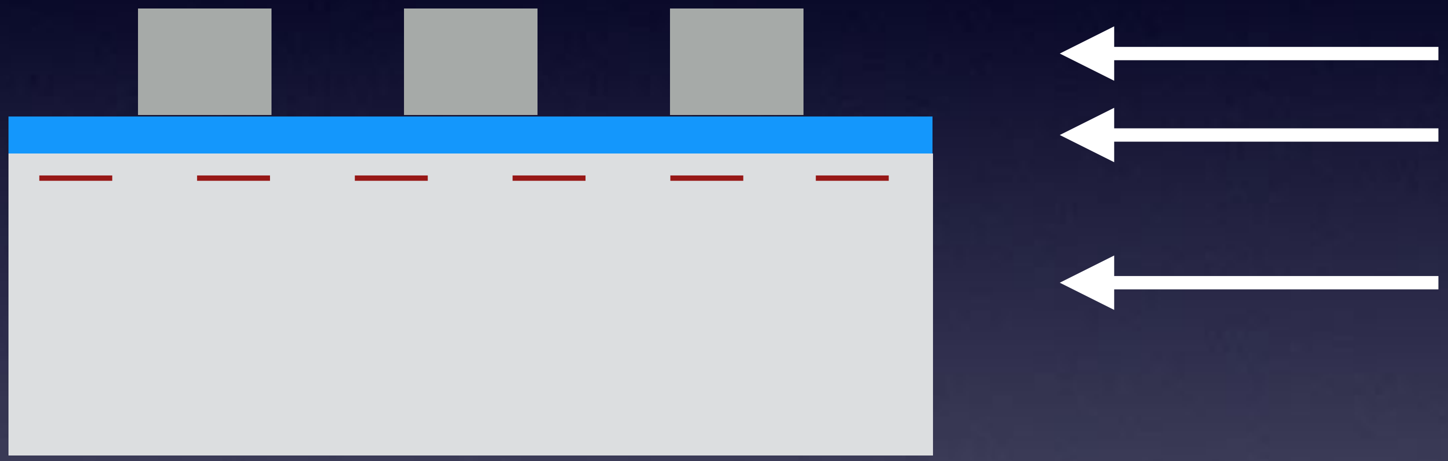
C. King, J.S. Schoenfield, M.J. Calderón, B.Koiller, A. Saraiva, X. Hu,
HW Jiang, M. Friesen, S.N. Coppersmith, arXiv:1807.11064

- Improving control of valley splitting in Si/SiGe heterostructures by modifying the materials stack

S.F. Neyens, R.H. Foote, B. Thorgrimsson, T.J. Knapp, T. McJunkin, L.M.K. Vandersypen, P. Amin, N.K. Thomas, J.S. Clarke, D.E. Savage, M.G. Lagally, M. Friesen, S.N. Coppersmith, M.A. Eriksson, *Appl. Phys. Lett.* **112**, 243107 (2018).

Si/SiGe heterostructures versus Si MOS: Oxide defects versus control of valley physics

Which problem is easier to solve?

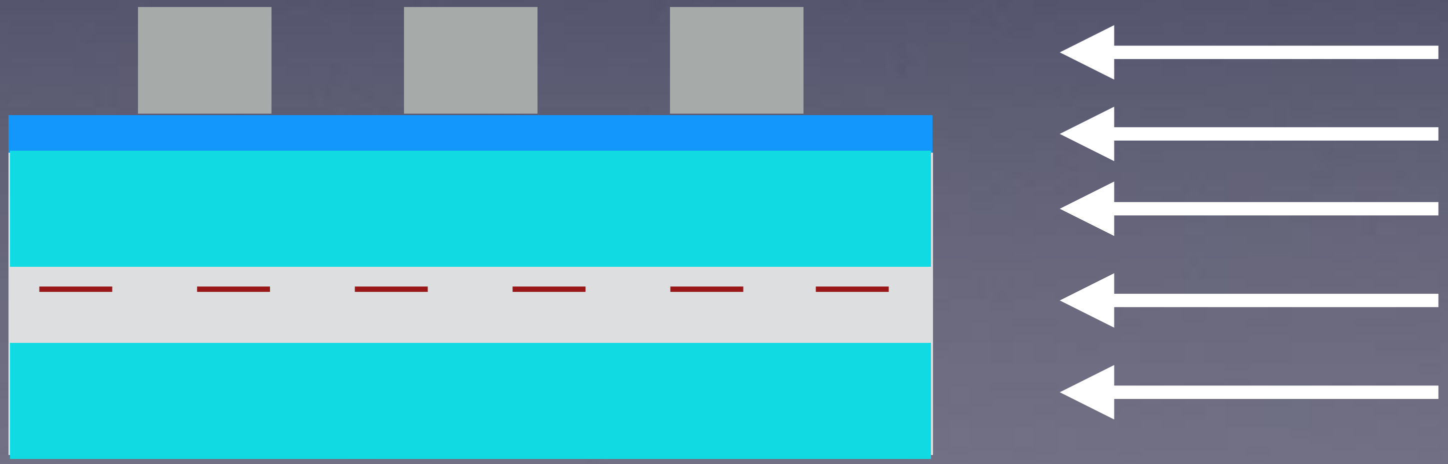


metal gates

oxide (a few nm)

silicon

electrons are close to defects in the oxide



metal gates

oxide (a few nm)

silicon-germanium

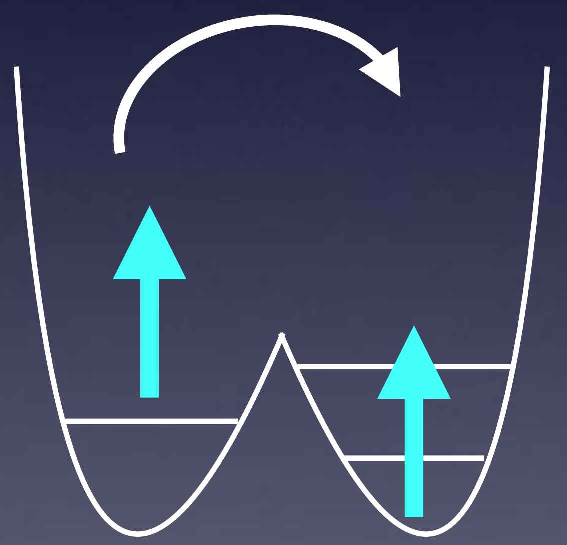
silicon

silicon-germanium

valley splitting tends to be harder to control

Si MOS devices: Defects in oxide complicate behavior

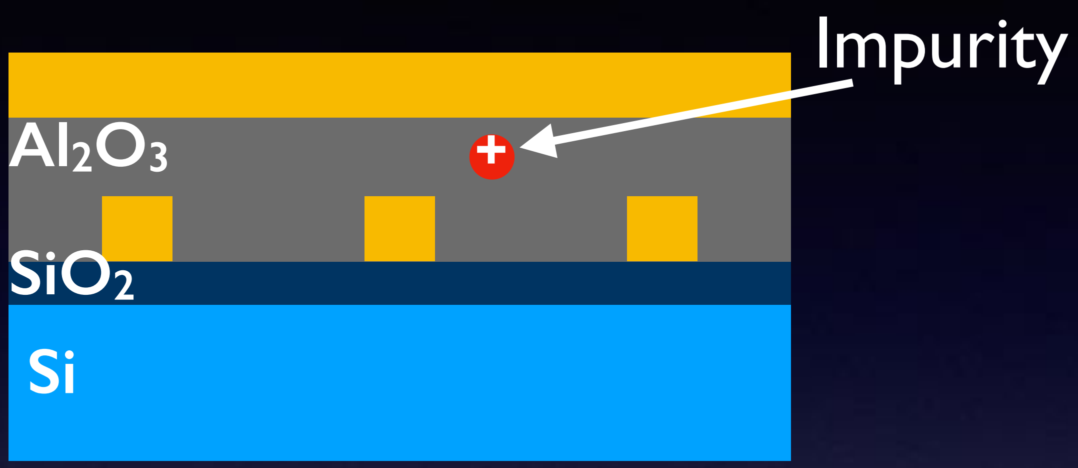
A large fraction of Si MOS quantum dot devices unexpectedly fail to exhibit "spin blockade" (apparent violation of Pauli exclusion principle)

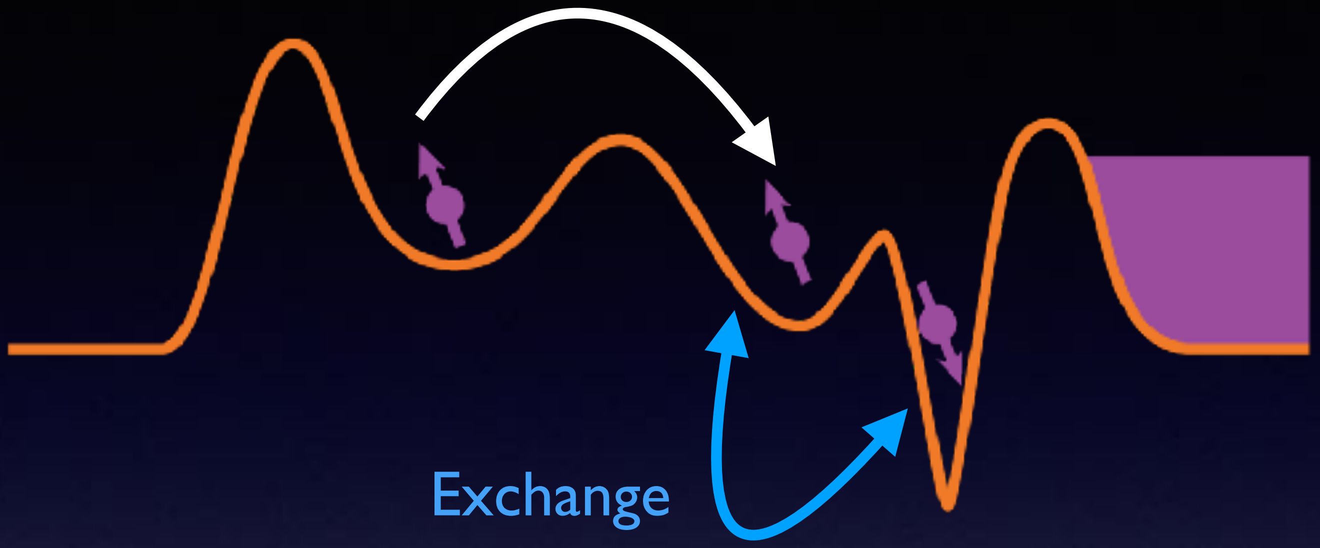


Natural explanation: defect induces impurity level with another electron.

C. King, J.S. Schoenfield, M.J. Calderón, B.Koiller, A. Saraiva, X. Hu, HW Jiang, M. Friesen, S.N. Coppersmith, arXiv:1807.11064

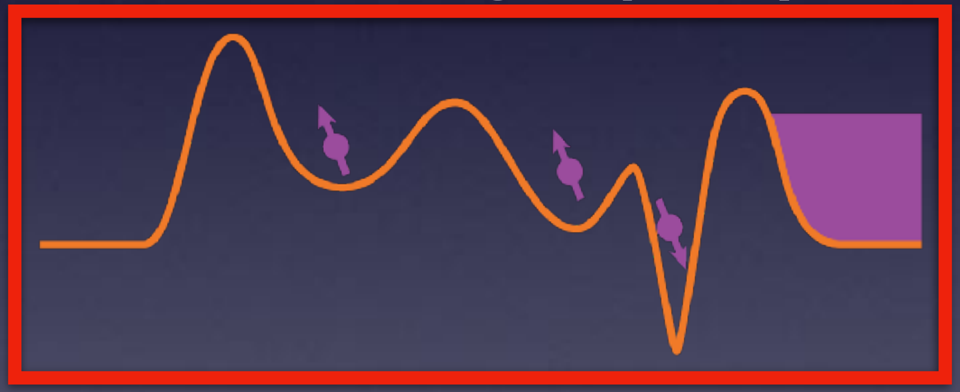
Spin blockade in Si-MOS devices can be lifted via impurity-induced dots strongly coupled to lithographic dots



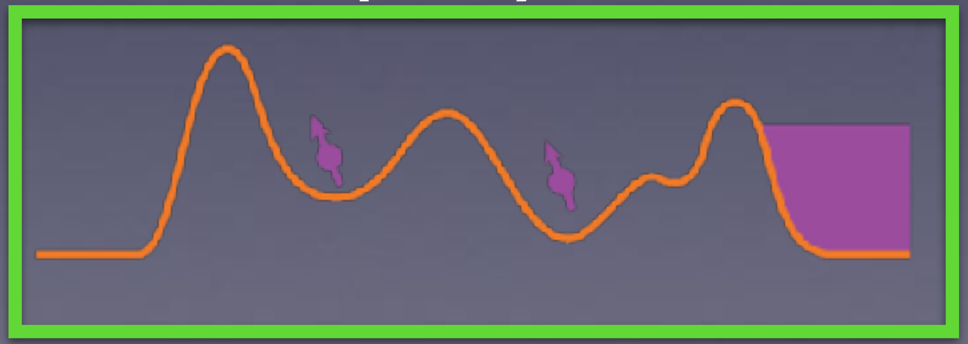


- <u>Impurity-induced dot requirements:</u>
    - Deep (1.0 meV) induced bound state level to avoid emptying during device tune up
    - Strong exchange coupling (>200 MHz) to nearby lithographic dot to allow random spin flips during singlet-triplet experiments

Spin blockade lifting impurity location



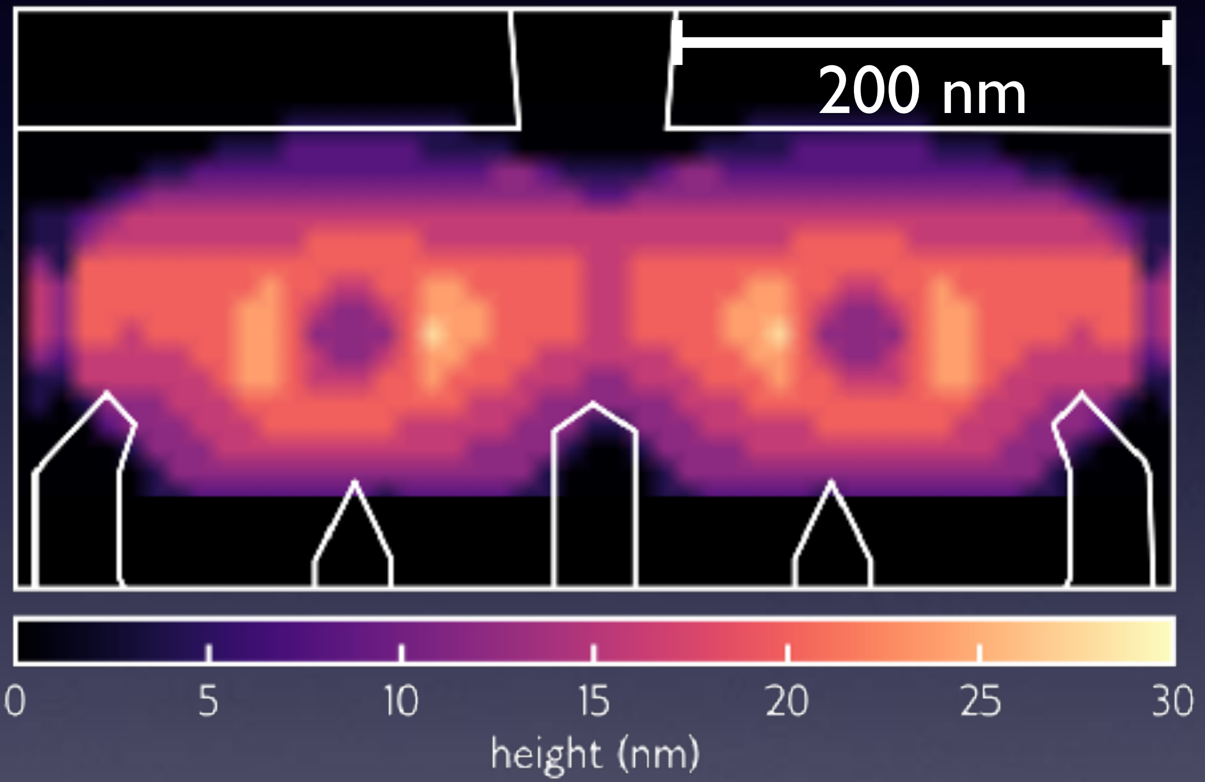
Safe impurity location



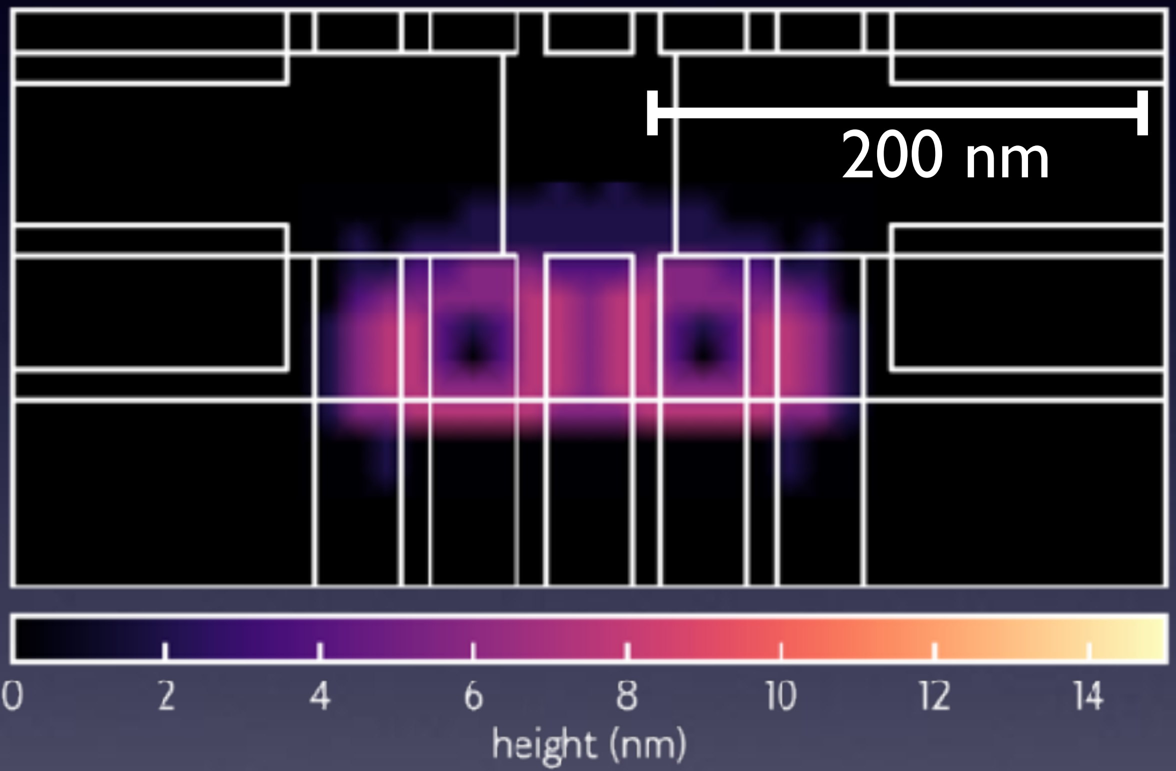
C. King, J.S. Schoenfield, M.J. Calderón, B.Koiller, A. Saraiva, X. Hu, H.W. Jiang, M. Friesen, S.N. Coppersmith, arXiv:1807.11064

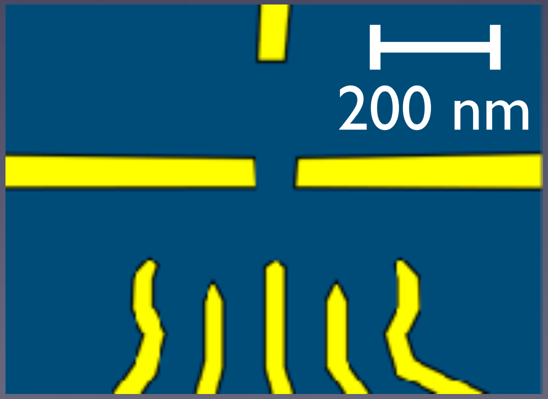
Volume of impurity locations leading to Pauli spin blockade (PSB) can be reduced by changing the device design so that screening of oxide layer is increased.

Volume of PSB lifting impurity locations:
Stadium-style device

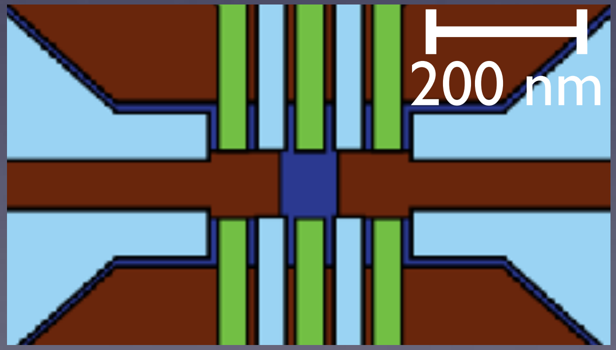


Volume of PSB lifting impurity locations:
Overlapping-style device



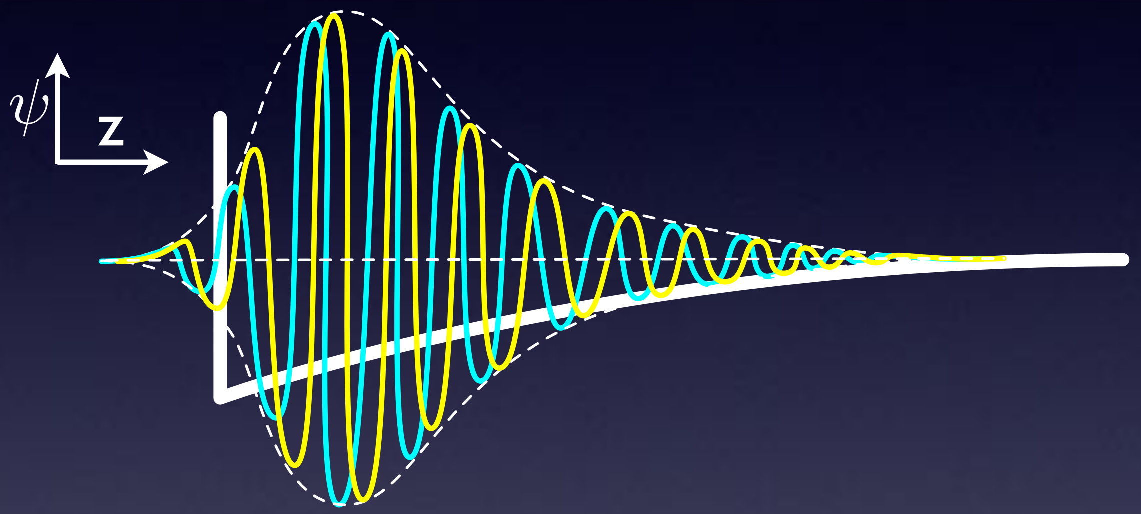


Overlapping gate devices allow for a large reduction in the volume of impurity locations that lead to an impurity-induced dot that lifts spin blockade



C. King, J.S. Schoenfield, M.J. Calderón, B.Koiller, A. Saraiva, X. Hu, HW Jiang, M. Friesen, S.N. Coppersmith, arXiv:1807.11064

SiGe heterostructure: need to improve control of the valley splitting of the electrons in the silicon quantum well.



Electron wavefunction perpendicular to quantum well oscillates with period ~ 1 nm.

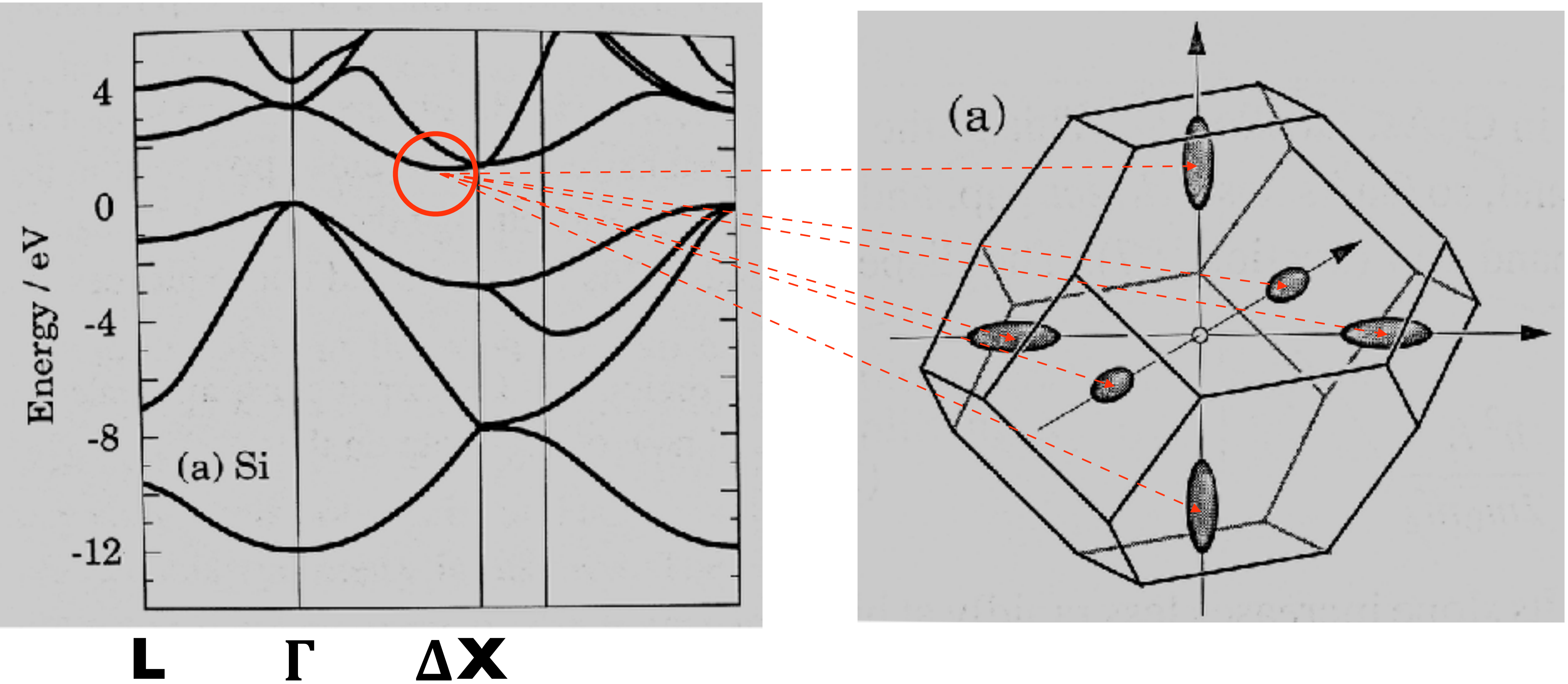
The properties of the two valley states are very sensitive to disorder at the quantum well interface.

Need to control valley splitting — typically make it large enough so that valley states are well-separated fom qubit subspace

Valleys in Si

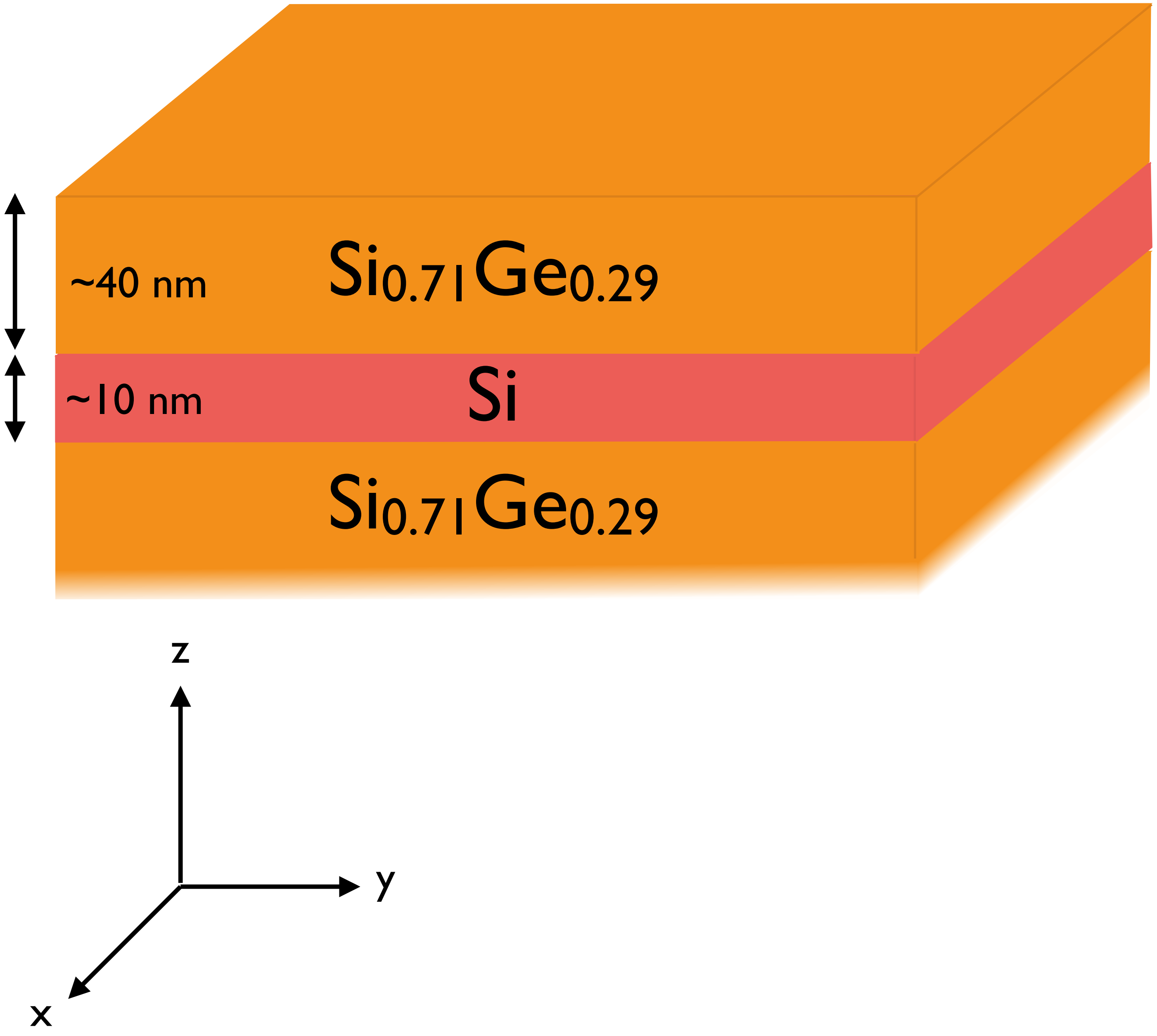
Si band structure

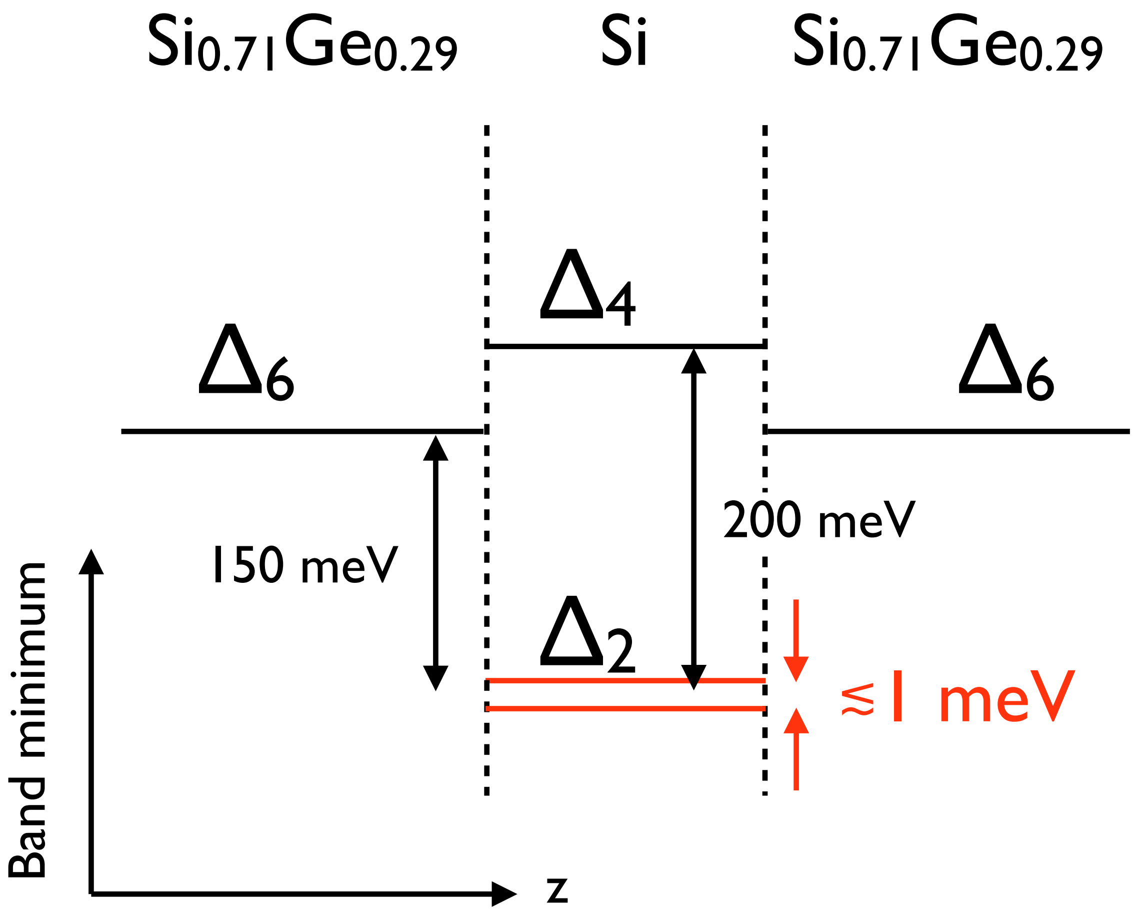
Constant energy surfaces above conduction band minimum (k-space)



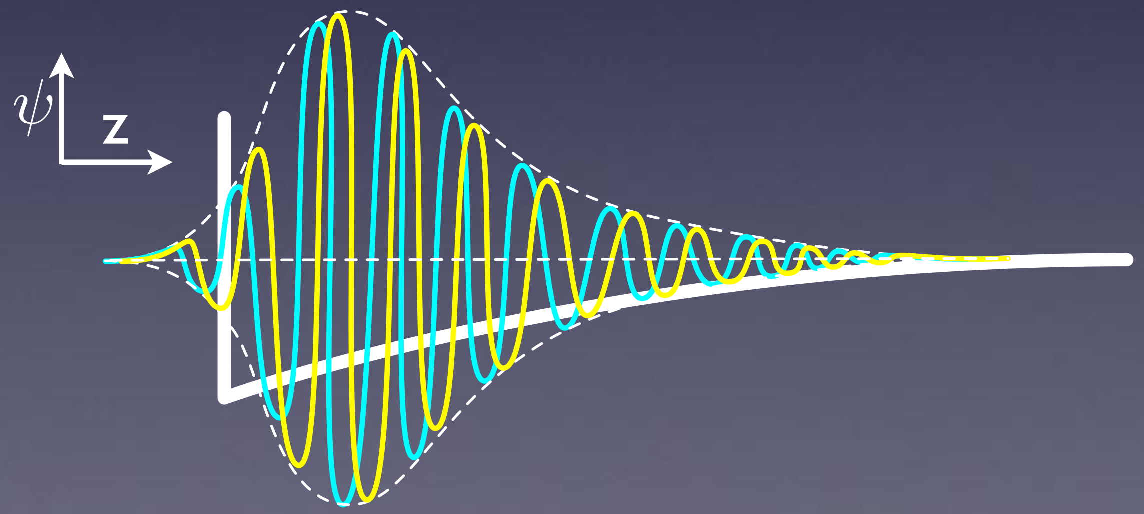
Images: John H. Davies, *The Physics of Low-Dimensional Semiconductors*, Cambridge University Press (2000)

Tensile strain in quantum well increases energy of 4 of the valleys, leaving two low-energy ±z valleys



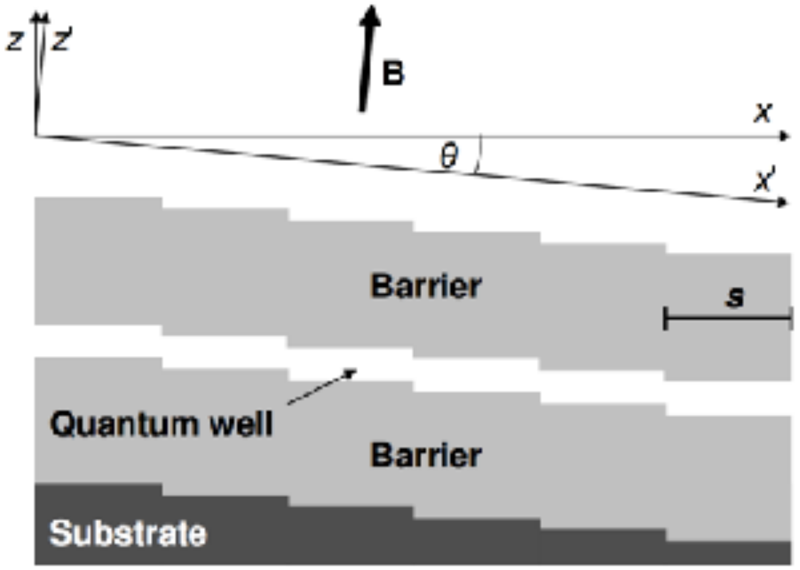


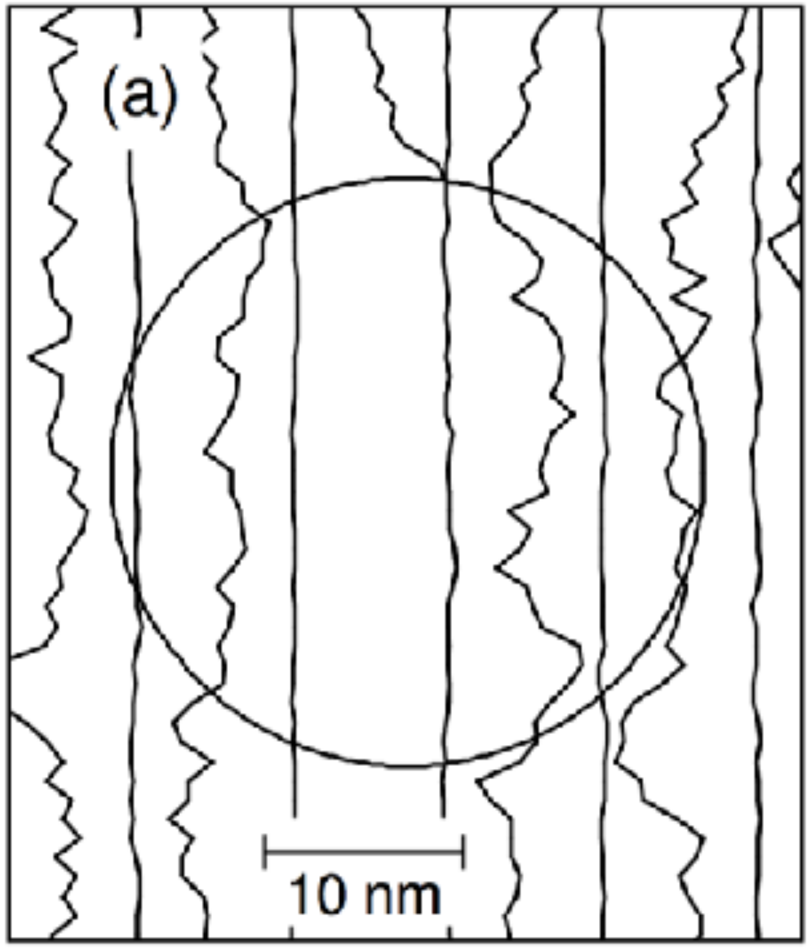
Splitting of ±z valleys is induced by jump in composition plus application of electric field



Increasing germanium concentration at interface increases the band offset between Si and SiGe, but tends to lower interface quality, which decreases valley splitting.

Heterostructure imperfections can suppress valley splitting significantly





- Valley splitting in a quantum well can be large (~1 meV or ~240 GHz)
  - Requires ideal quantum well interface (uniform, infinitely sharp)
- In real samples, valley splitting is suppressed by non-uniformity
- Confinement improves valley splitting

Mark Friesen, M.A. Eriksson, and S. N. Coppersmith. Appl. Phys. Lett. **89**, 202106 (2006)

Quantitative understanding of valley splitting requires a multiscale approach.

(Valley splitting arises from atomic-scale physics, but want to use continuum equations to determine wavefunctions.)

S. Chutia, S.N. Coppersmith and M. Friesen, "Multiscale theory of valley splitting in the conduction band of a quantum well," *Physical Review B* **77**, 193311 (2008) implements a multiscale implementation of a one-dimensional model.

But need to incorporate the effecs of interface steps for the theory to be really useful for experiments.

Here, will discuss experimental measurements.

Strategy for improving control of valley splitting:

See if more complex materials stack for Si/SiGe heterostructures can make valley splitting larger and more controllable.

Motivation:
theoretical proposal by Zhang et al. (2013)

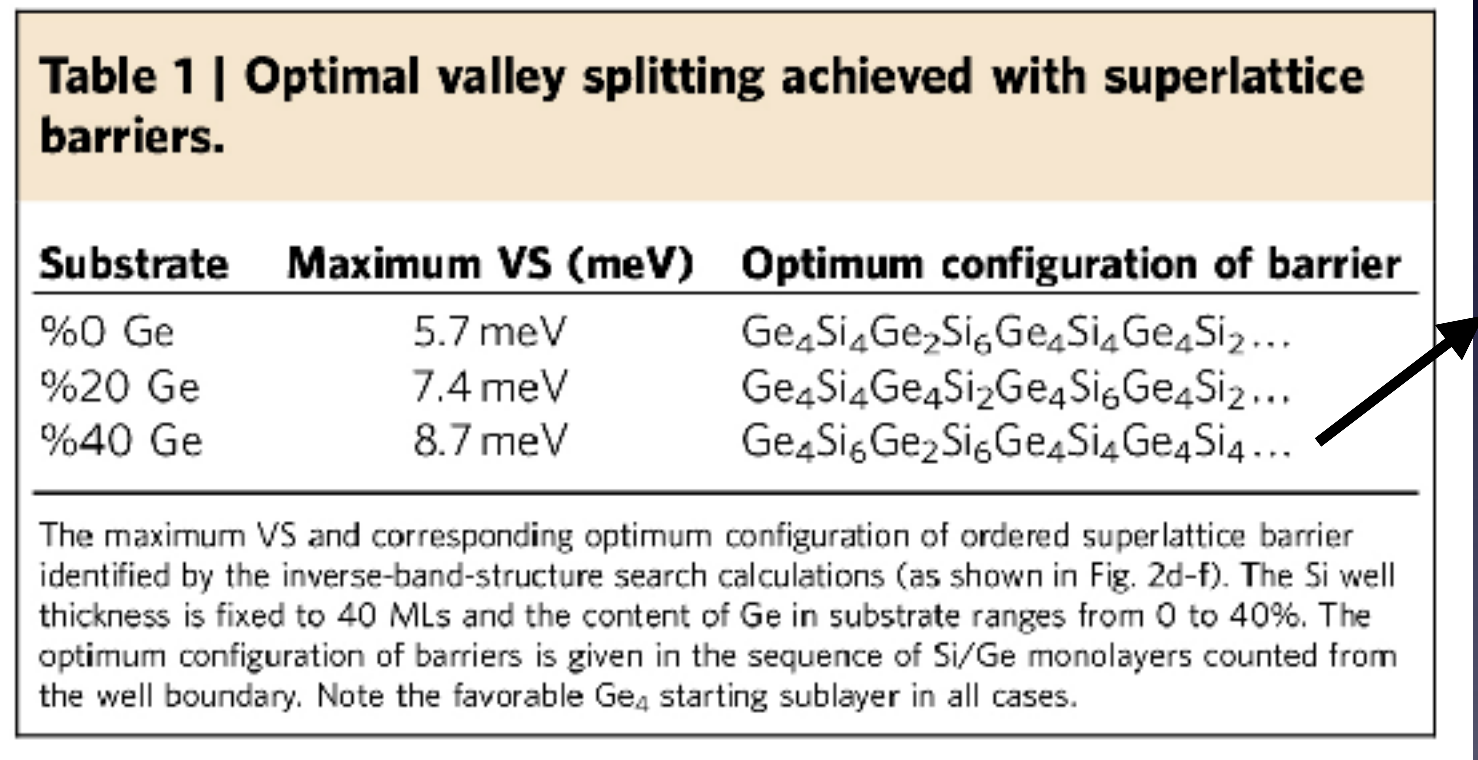
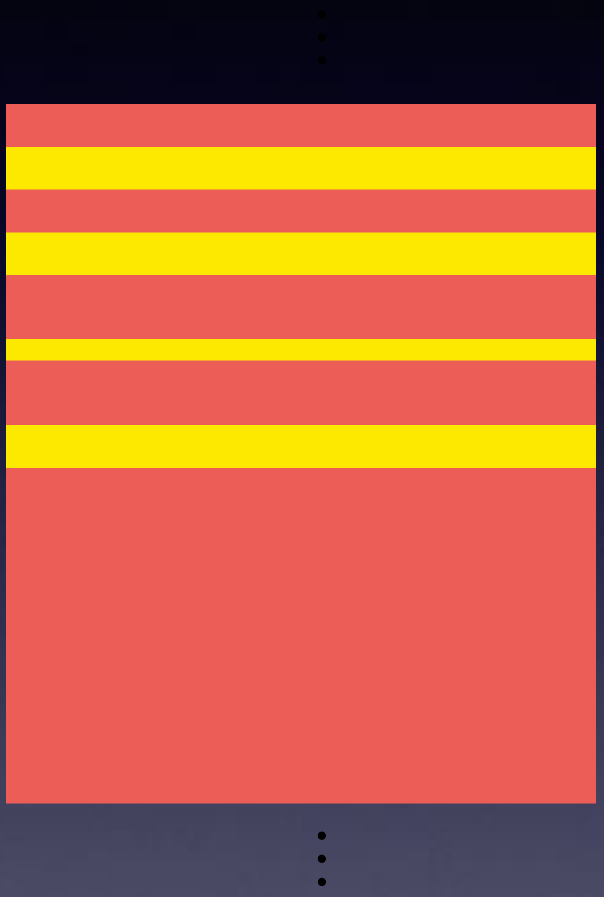


Table 1 | Optimal valley splitting achieved with superlattice barriers.

Substrate	Maximum VS (meV)	Optimum configuration of barrier
%0 Ge	5.7 meV	$Ge_4Si_4Ge_2Si_6Ge_4Si_4Ge_4Si_2\ldots$
%20 Ge	7.4 meV	$Ge_4Si_4Ge_4Si_2Ge_4Si_6Ge_4Si_2\ldots$
%40 Ge	8.7 meV	$Ge_4Si_6Ge_2Si_6Ge_4Si_4Ge_4Si_4\ldots$

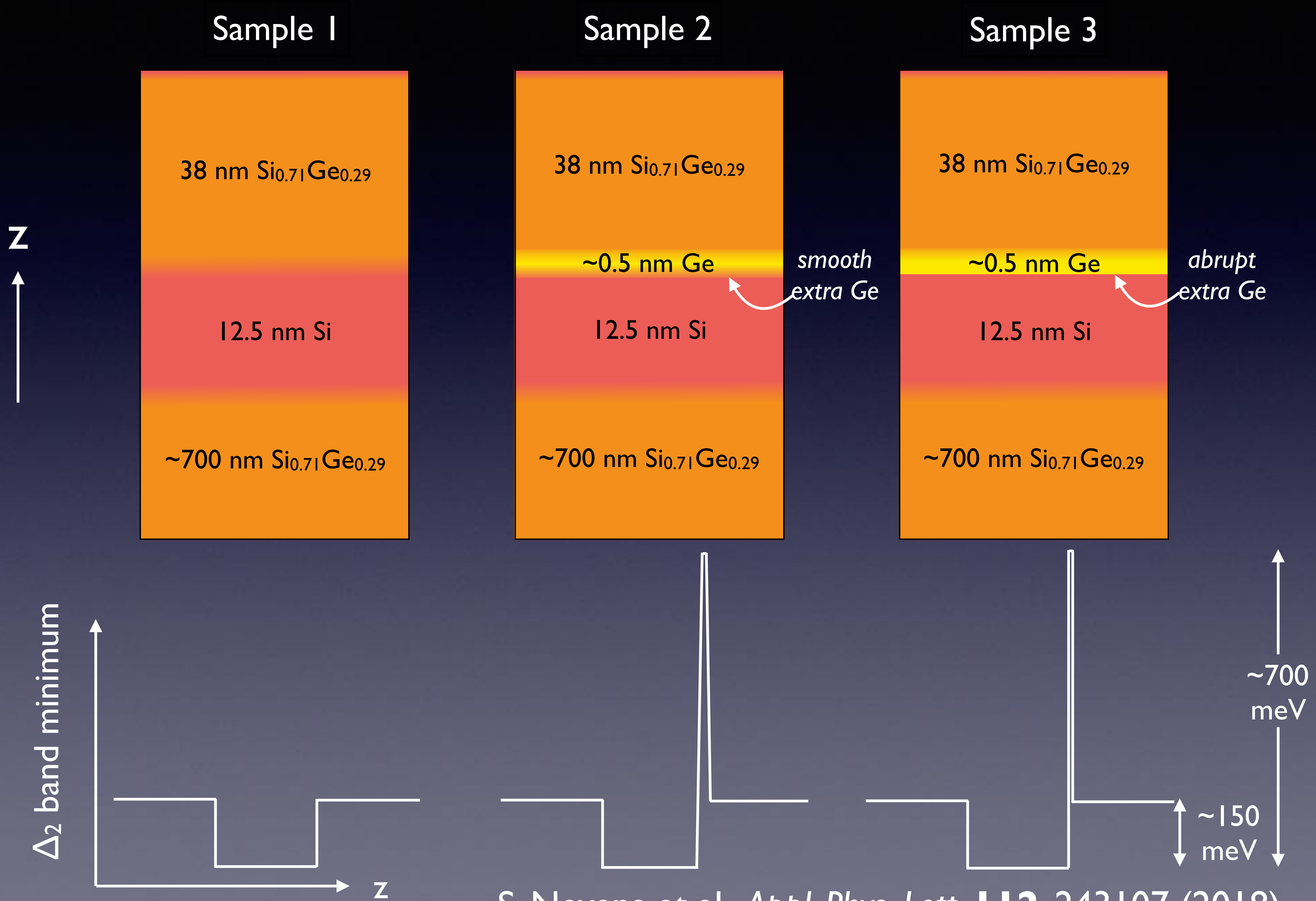
The maximum VS and corresponding optimum configuration of ordered superlattice barrier identified by the inverse-band-structure search calculations (as shown in Fig. 2d-f). The Si well thickness is fixed to 40 MLs and the content of Ge in substrate ranges from 0 to 40%. The optimum configuration of barriers is given in the sequence of Si/Ge monolayers counted from the well boundary. Note the favorable Ge_4 starting sublayer in all cases.



L. Zhang J.W. Luo, A. Saraiva, B. Koiller, A. Zunger,
Nature Comm. **4**, 2396 (2013)

Our work: One additional 0.5 nm layer of Ge near surface of quantum well
S. Neyens et al., *Appl. Phys. Lett.* **112**, 243107 (2018).

Three heterostructures were studied, one control and two with enhanced germanium at the quantum well interface



S. Neyens et al., *Appl. Phys. Lett.* **112**, 243107 (2018)

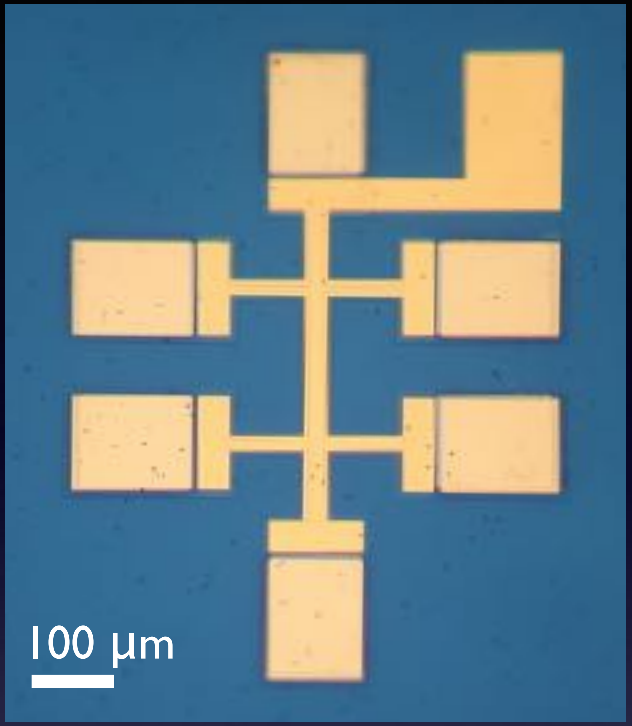
Adding the Ge monolayer increases band offset (which raises valley splitting), but it also can decrease disorder at the interface (which lowers valley splitting).

Sample	Mobility ($cm^2V^{-1}s^{-1}$) at carrier density $n=4\times10^{11}$
control	100,000
“smooth” extra Ge	70,000
“abrupt” extra Ge	56,000

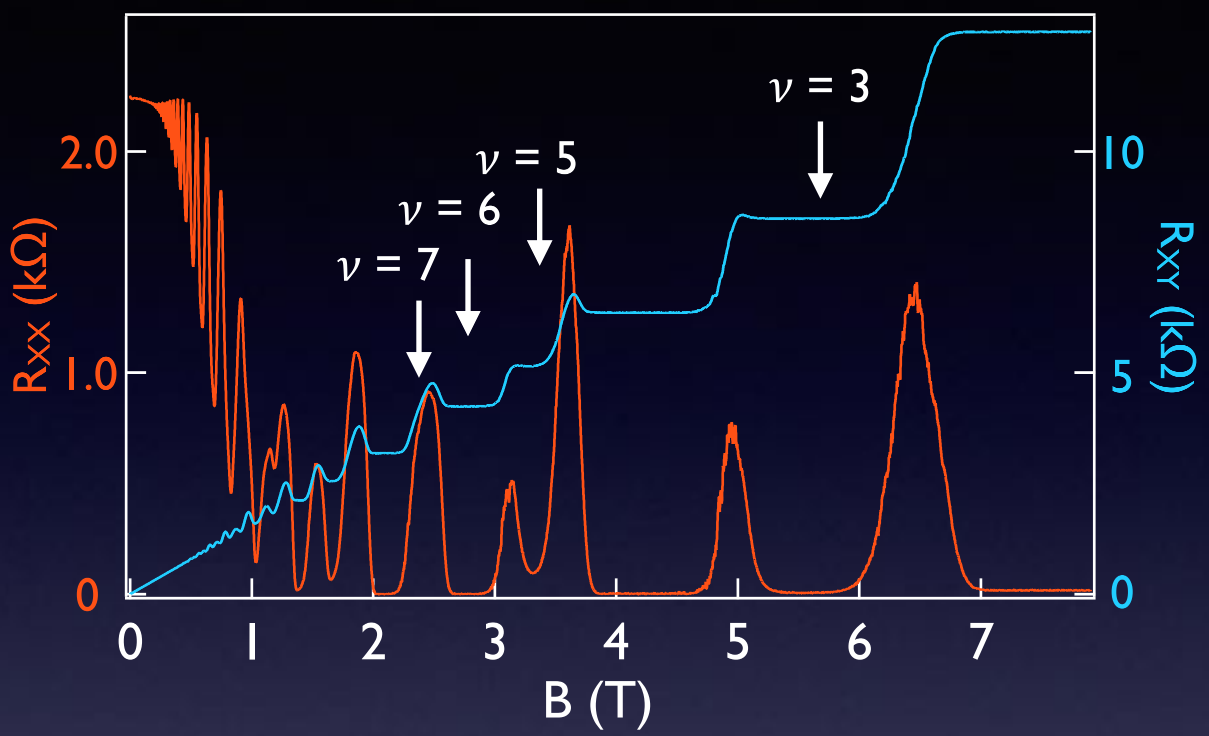
Heterostructures with extra Ge at interface have somewhat lower mobilities, indicating that the interfaces are somewhat more disordered.

So need to measure the valley splittings!

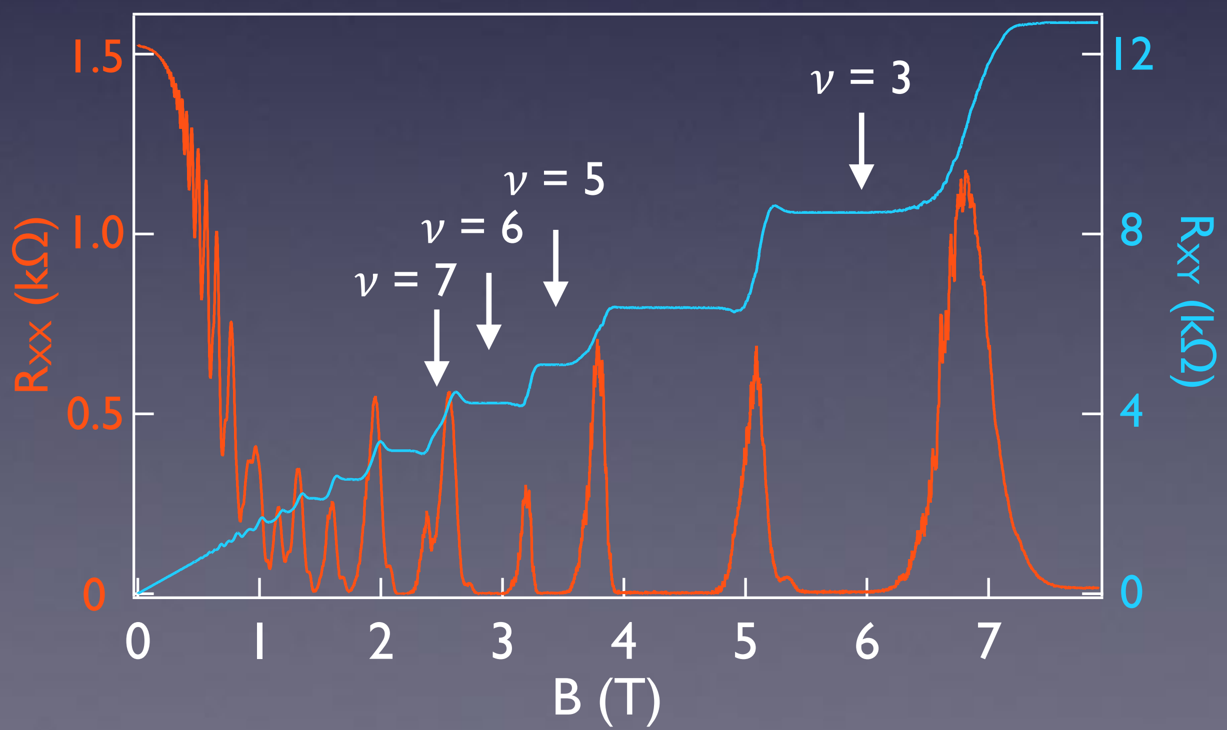
Temperature dependence of quantum Hall measurements are used to determine valley splittings as a function of carrier density, magnetic field.



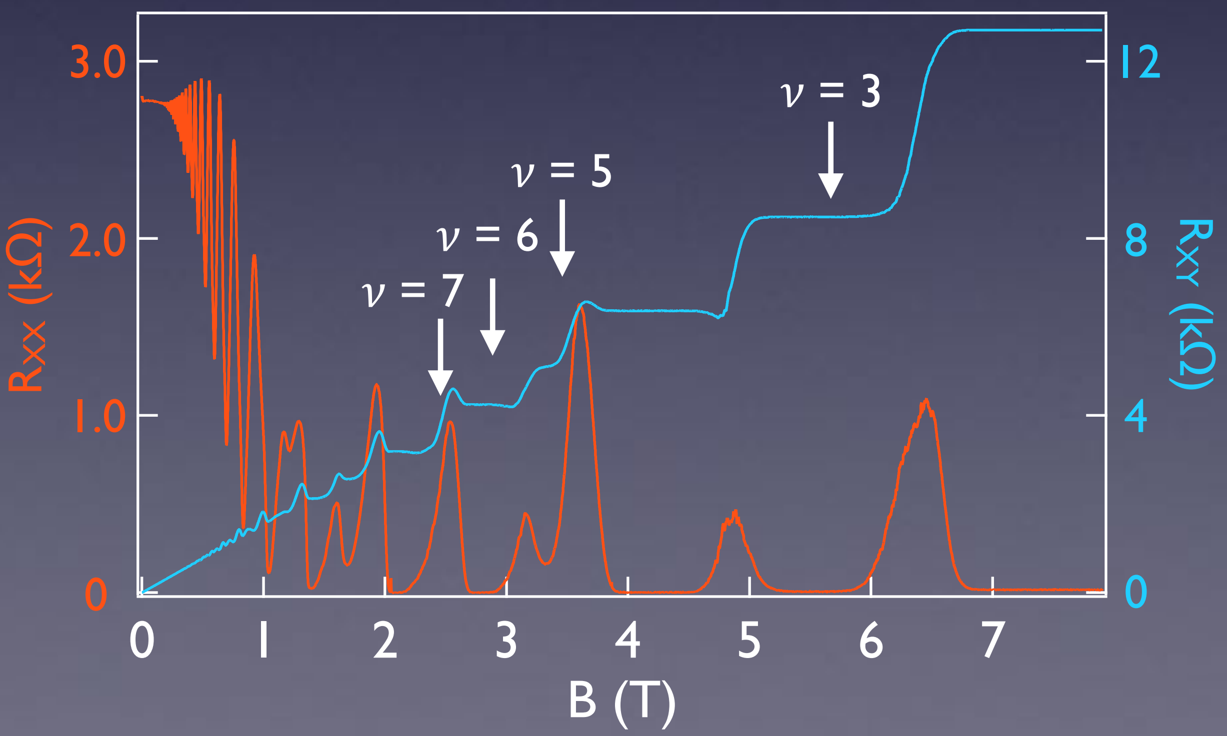
Smooth extra-Ge (Ge-1)



Control sample (Std.)

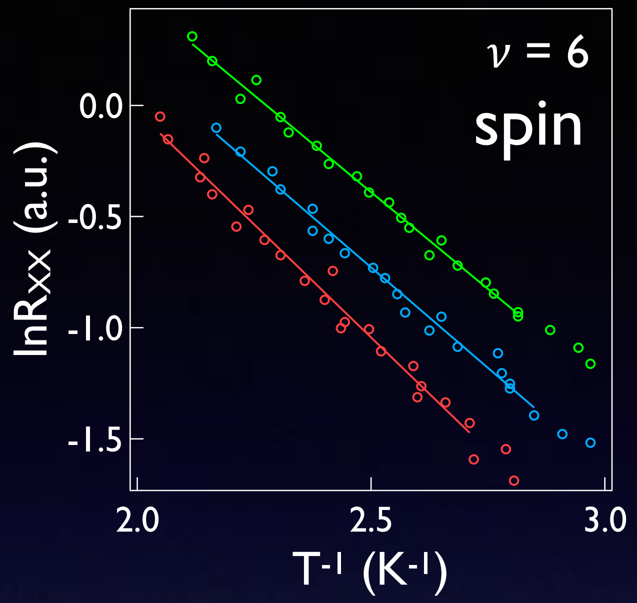


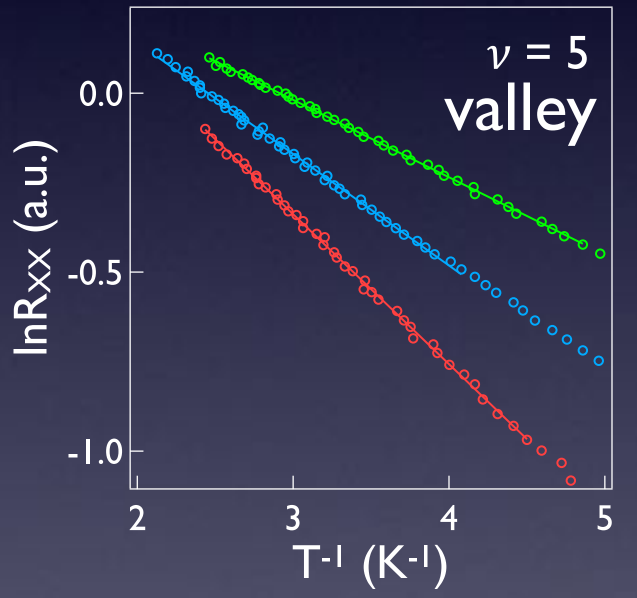
Abrupt extra-Ge (Ge-2)

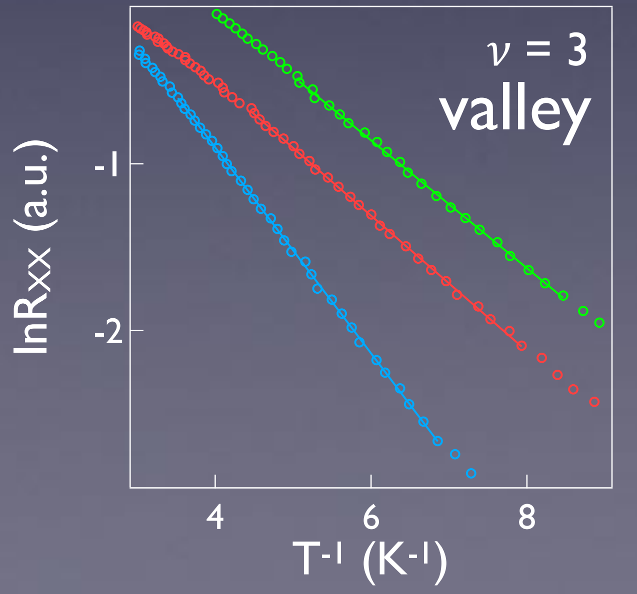


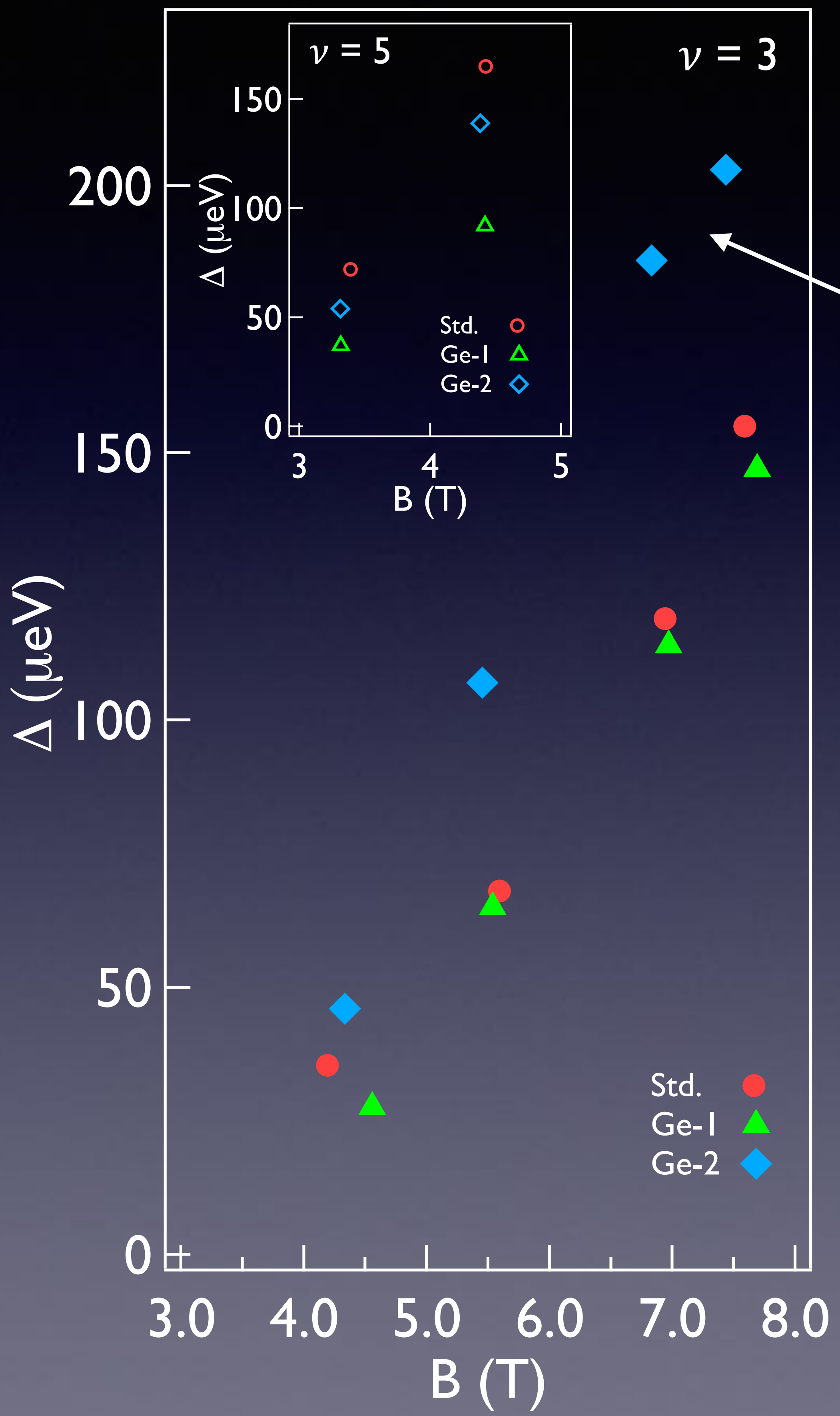
S. Neyens et al., *Appl. Phys. Lett.* **112**, 243107 (2018)

Results of thermal activation measurements to determine valley splittings at two different filling factors and different densities







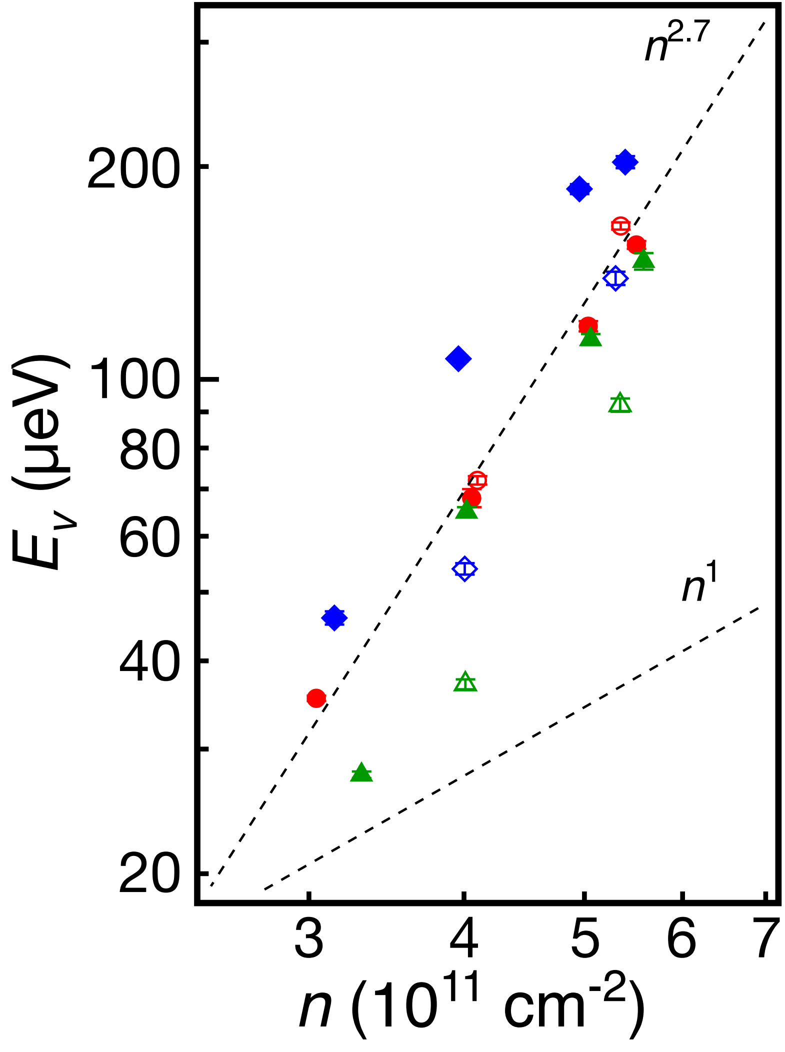


extra-Ge sample has enhanced valley splitting at this filling factor

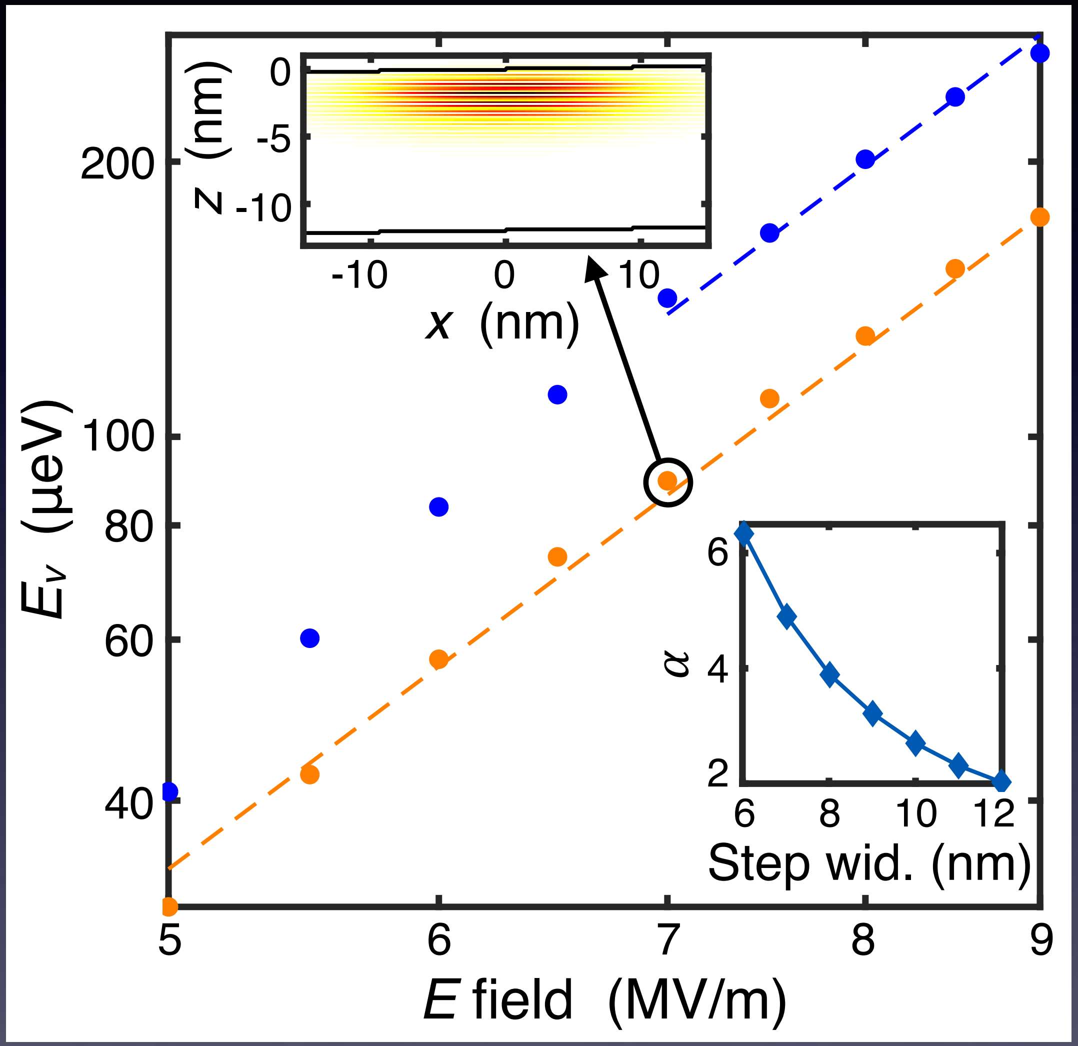
Uncertainty of linear fits is smaller than marker size

Experimental and theoretical valley splitting work agrees that disorder from the substrate can dominate over interface composition

Experiment:



Theory:



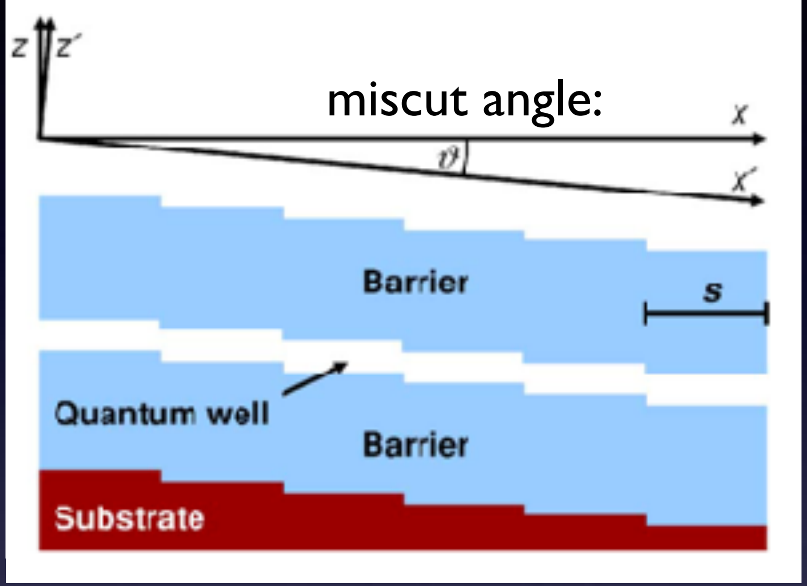
For all samples:

$E_V \sim n^{\alpha}$, $\alpha = 2.7 \pm 0.2$

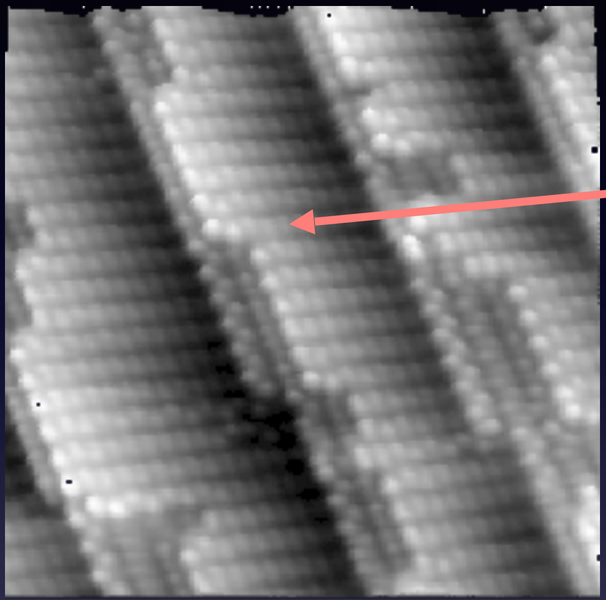
Tight binding simulations give the same scaling for a narrow range of step densities, indicating samples are more alike than they are different

S. Neyens, *et al.*, *Appl. Phys. Lett.* 112, 243107 (2018)

Heterostructures were grown on different substrates to test the prediction that double-atom steps suppress valley splitting less than single-atom steps



Friesen, et al.,
Phys. Rev. B **75**, 115318 (2007)



Miscut tilt towards [110]

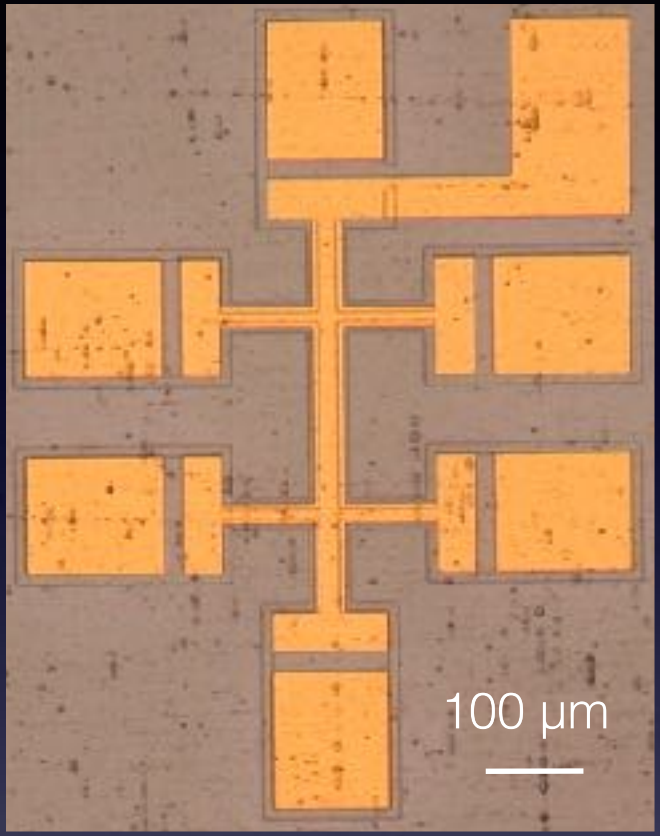
Lagally group archive

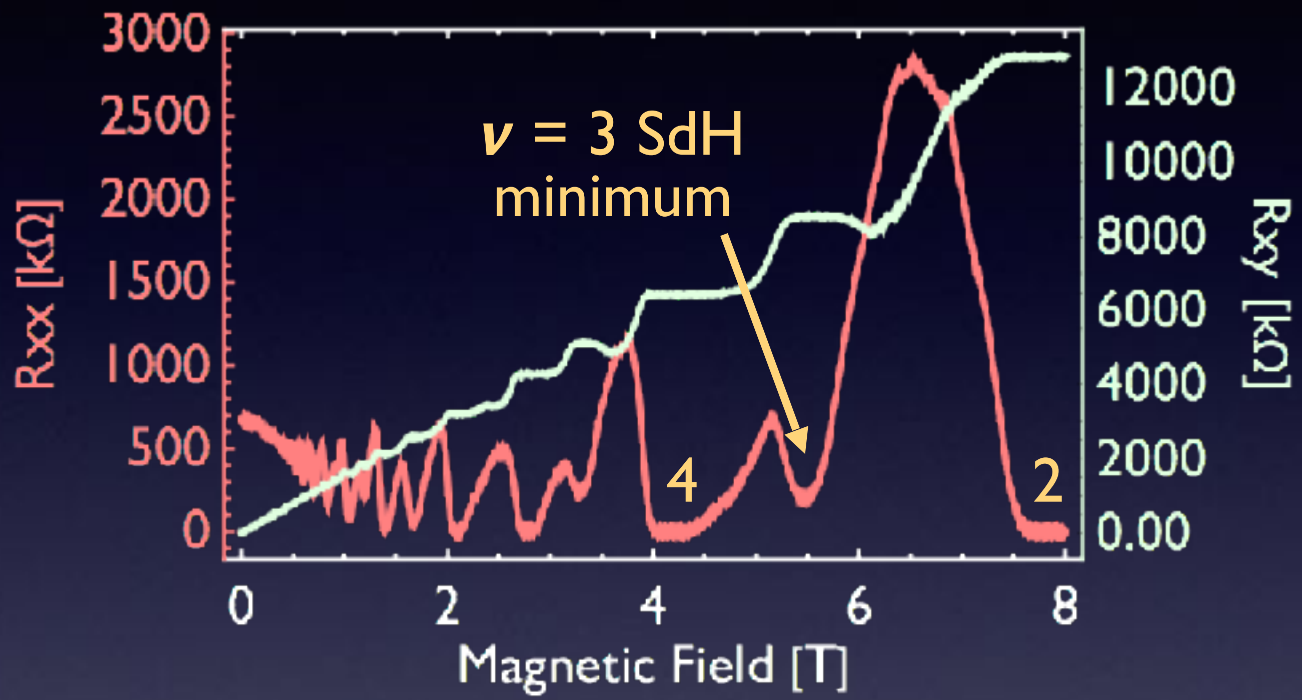
Three samples were grown by Don Savage on substrates with different miscuts, including

- A 2° miscut along [010], producing single-atom steps
- A 4° miscut along [110], producing two-atom steps* (with same average step width)
- An on-axis sample (no miscut), as a control

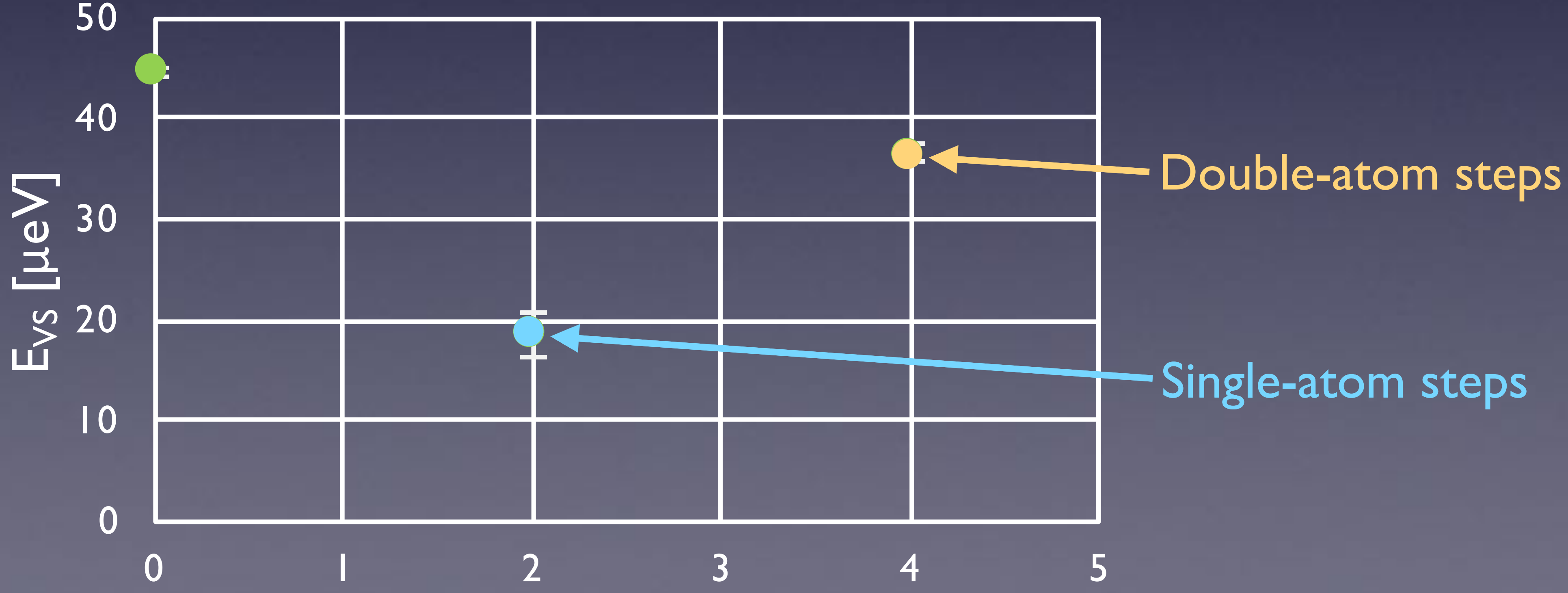
* J. E. Griffith, et al., *J. Vac. Sci. Technol. A* **7**, 1914 (1989)

Valley splitting was determined via thermal activation of Shubnikov-de-Haas minima in fields up to 8T.





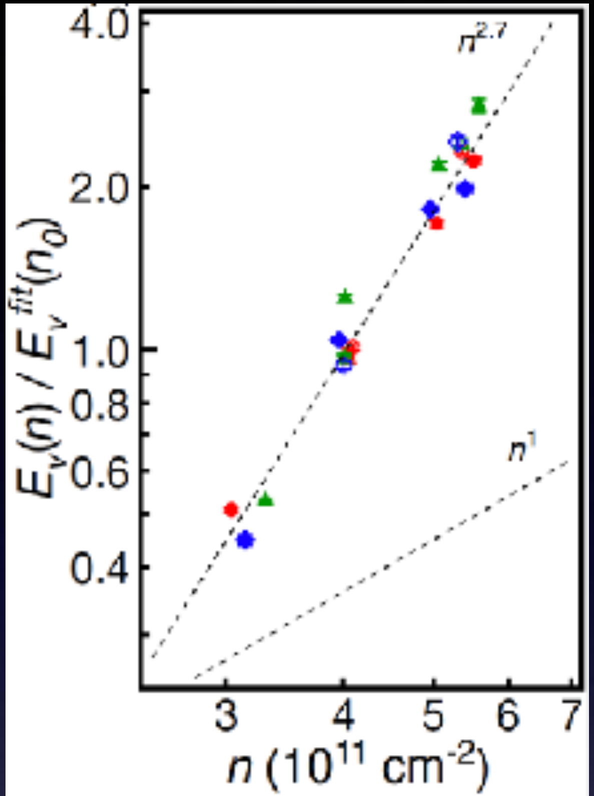
Good mobilities were observed at $n = 4 \times 10^{11}$ cm^{-2}, for all samples, in the range 150,000-250,000 cm^2/(V s)



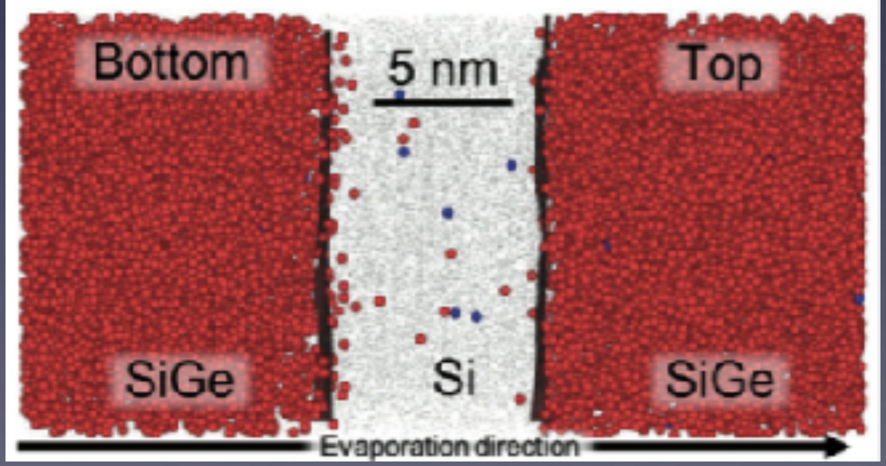
ν = 3 valley splitting at $n = 4 \times 10^{11}$ cm^{-2}

Tom McJunkin

Developing new heterostructures to enhance valley splitting

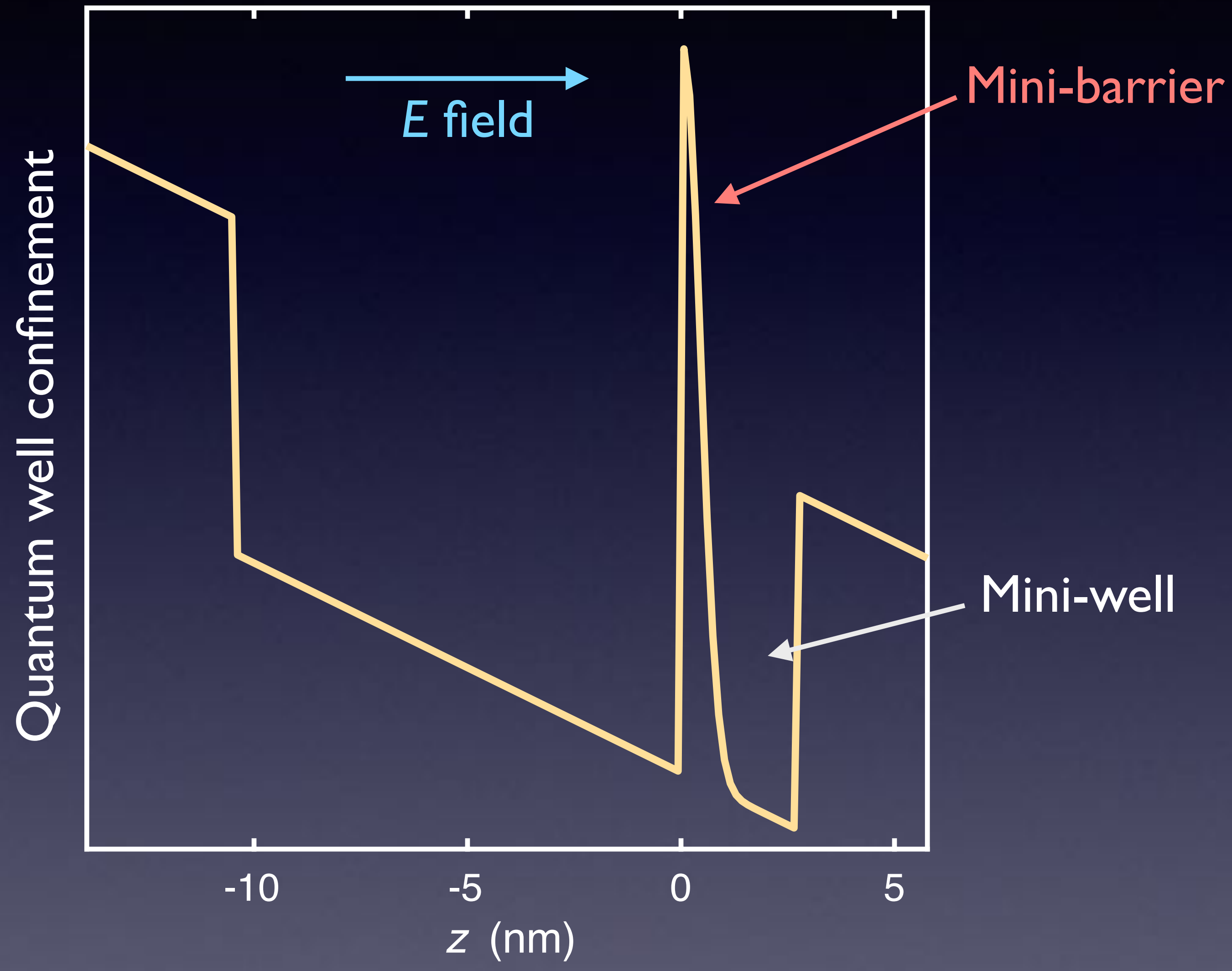


Observation #1: disorder is difficult to change. Think about the *structure*.



Atom probe: O. Dyck, et al., *Adv. Mater. Interfaces* **4**, 1700622 (2017).

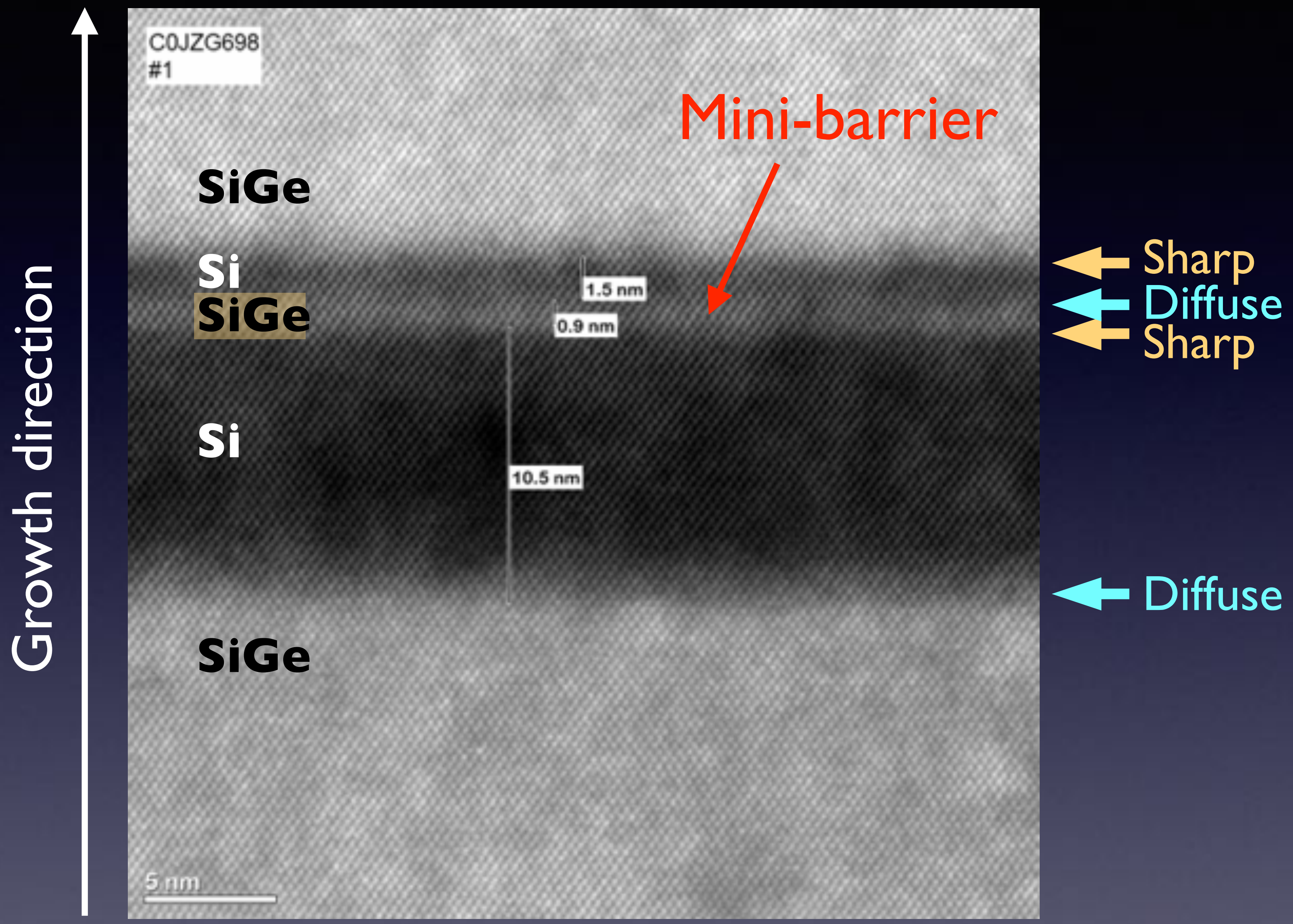
Observation #2: growth constraints provide *one sharp interface.*



Proposed solution: grow a very narrow, thin barrier near the top of the quantum well

Results of growth of mini-barrier

TEM image

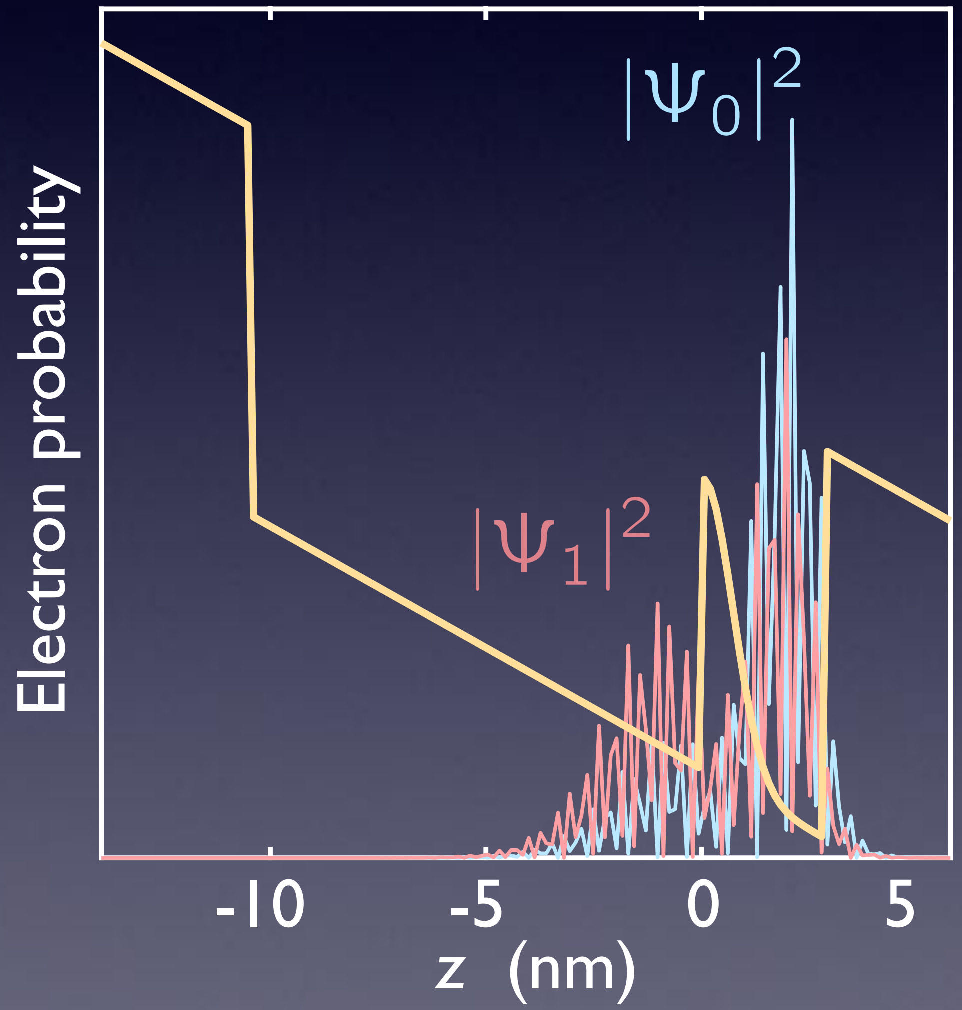


D. Savage

Ideal mini-barrier is narrow and sharp

Tight-binding simulations of mini-barriers

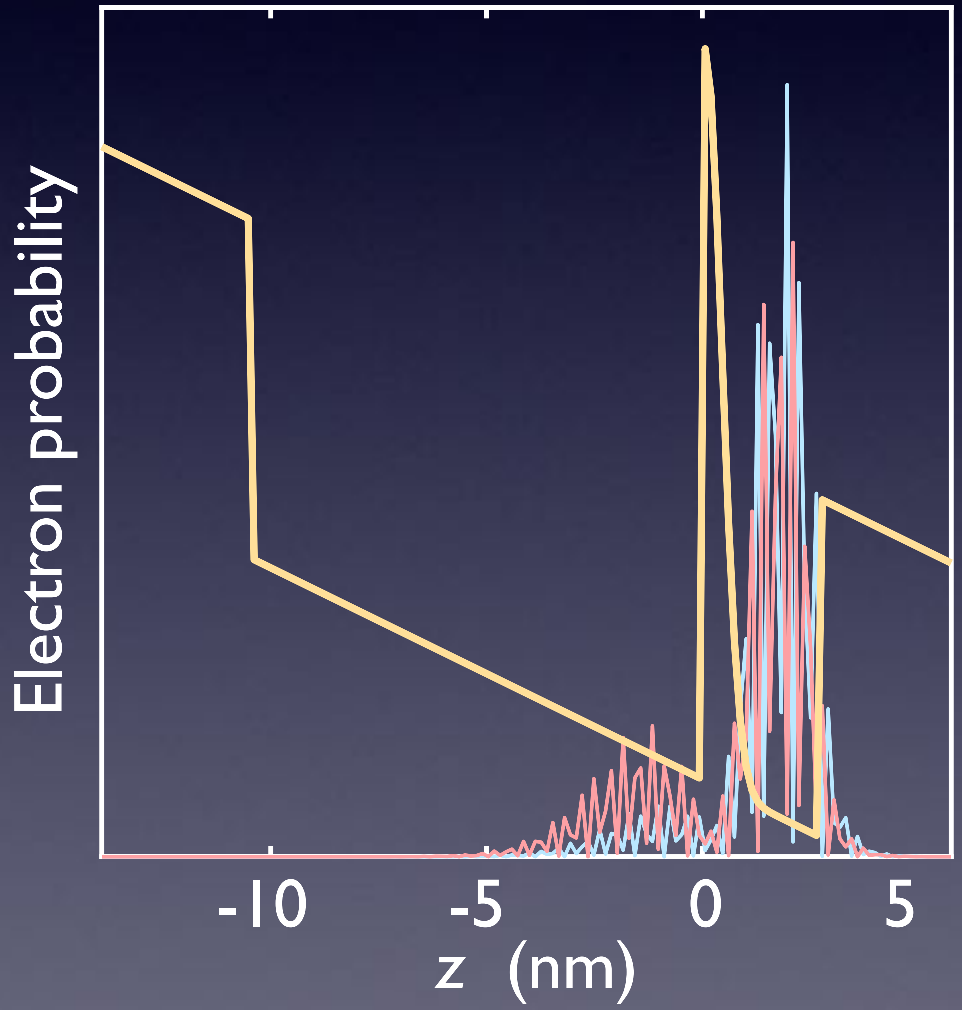
Half-Gaussian barrier model:



Predicted valley splitting enhancement factor (this structure): 1.34

We can do even better:

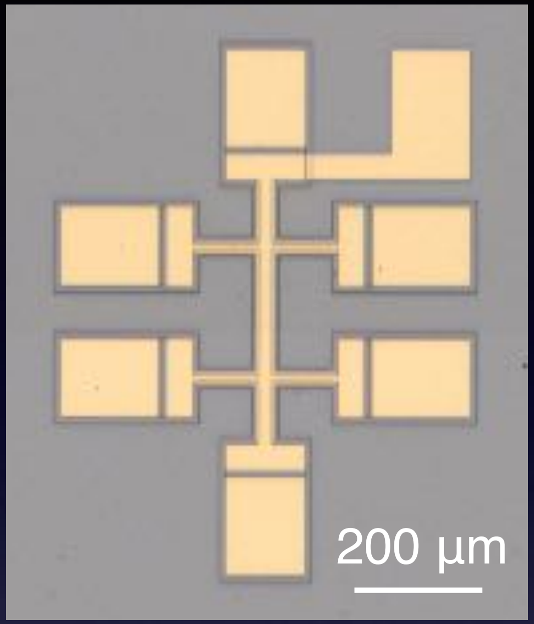
- sharper barriers
- higher Ge content

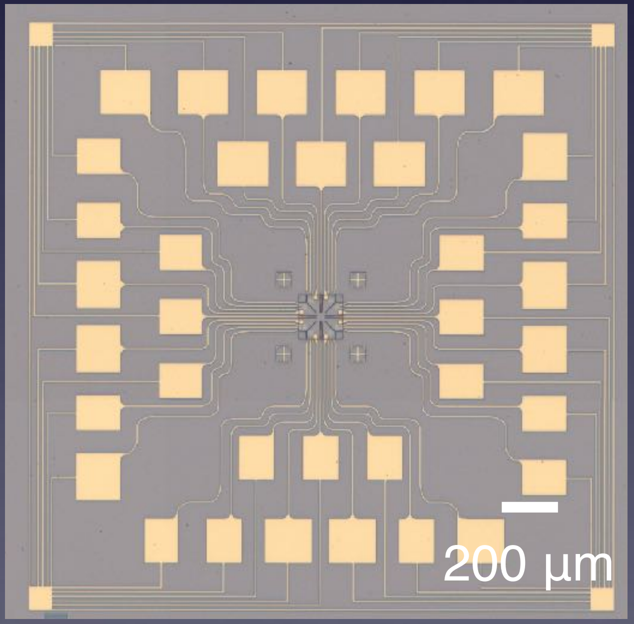


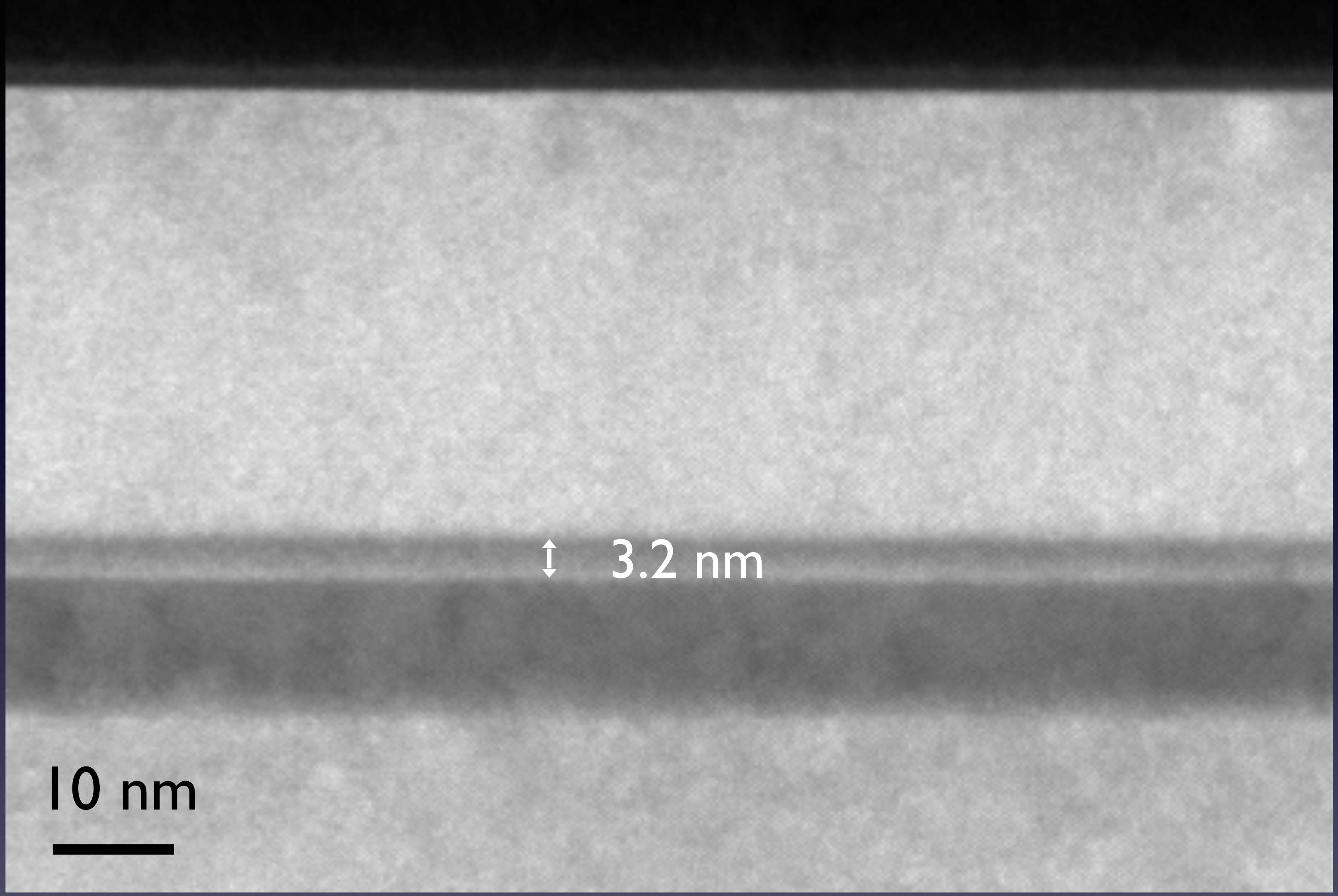
Predicted valley splitting enhancement factor: 3.2

Mark Friesen

Heterostructures grown with mini silicon layer above the quantum well to alter the overlap of the wave function into the SiGe barrier.







D. Savage

Dot and Hall bar fabrication is completed, valley splitting to be measured soon.

Tom McJunkin

Summary of quantum Hall effect measurements of valley splittings:

“Abrupt” extra-Ge sample exhibits systematically larger valley splittings at filling factor $\nu=3$ than the control and “smooth” extra-Ge sample.

Measurements at $\nu=5$ do not exhibit enhanced valley splitting for samples with extra Ge at interface.

(evidence that disorder and/or electron interactions could be playing an important role)

⇒ Need to conduct measurements in quantum dots

Summary

Silicon quantum dots are promising for quantum information processing.

Single-qubit gates with fidelities >99.9% have been demonstrated.

Two-qubit gates with fidelities >90% have been demonstrated.

Prospects for achieving higher fidelities and faster gate operations are good.

Improving materials is important to being able to scale up silicon quantum dot quantum computers.

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Thank you!

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S.F. Neyens et al., Appl. Phys. Lett. 112, 243107 (2018).